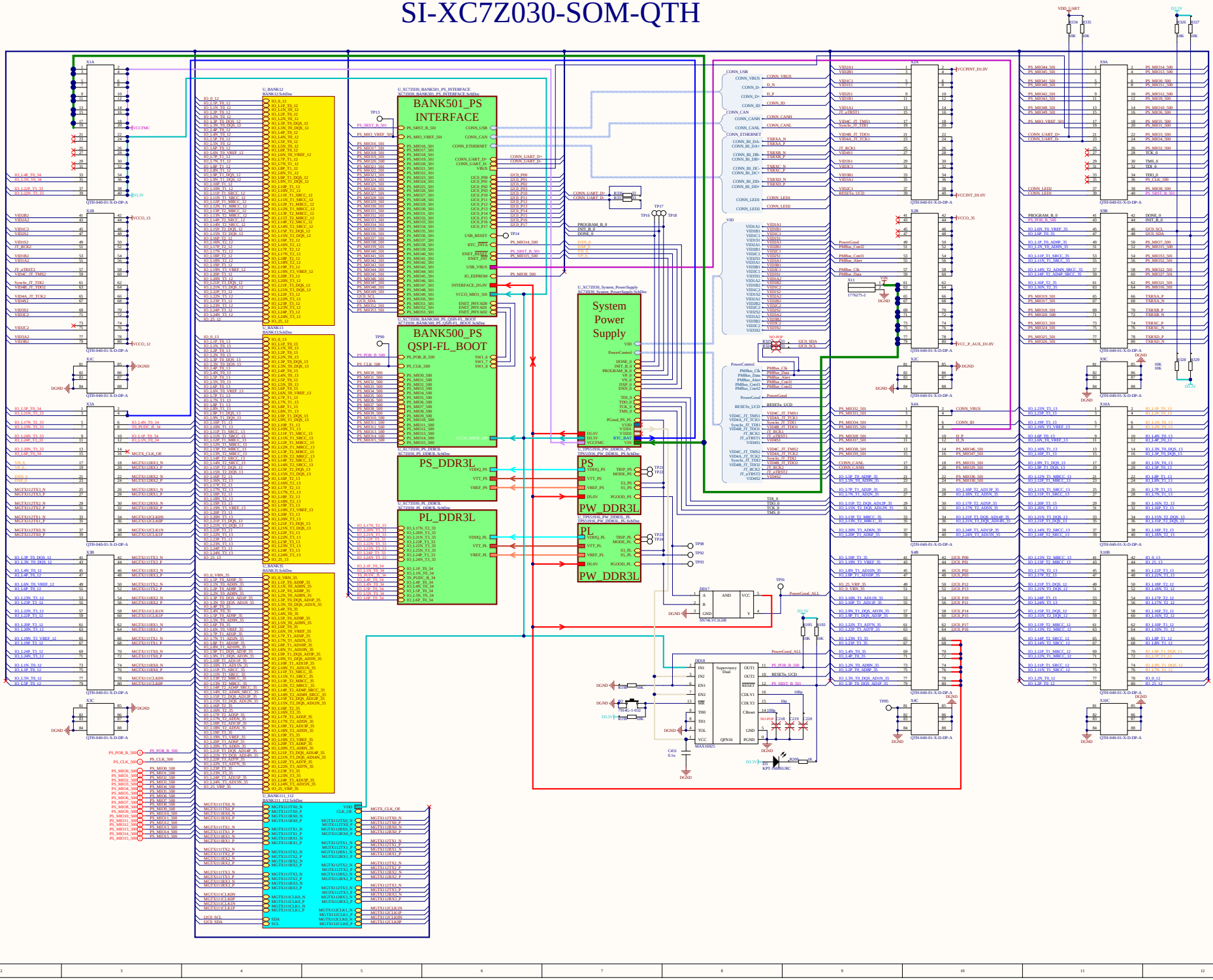
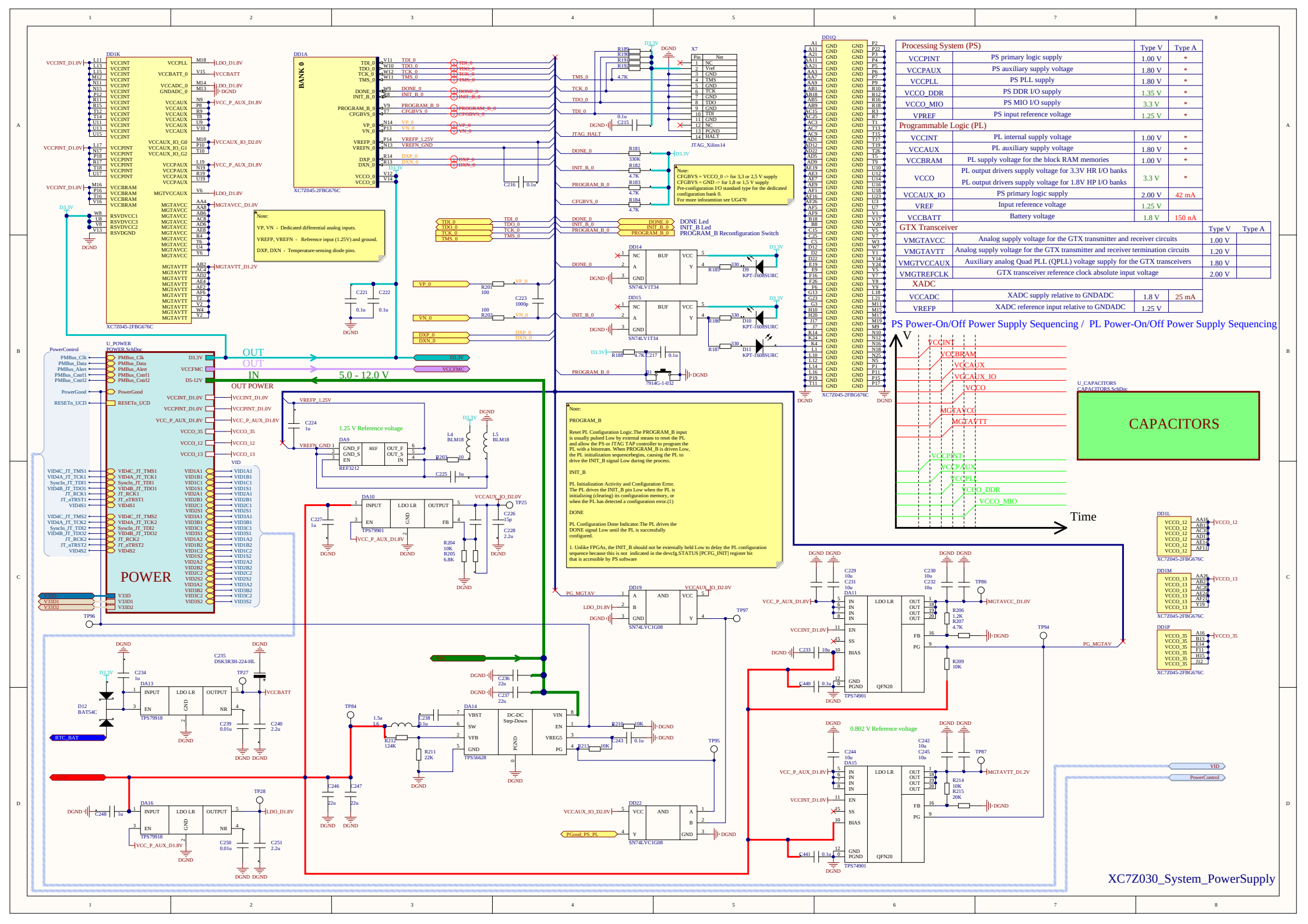
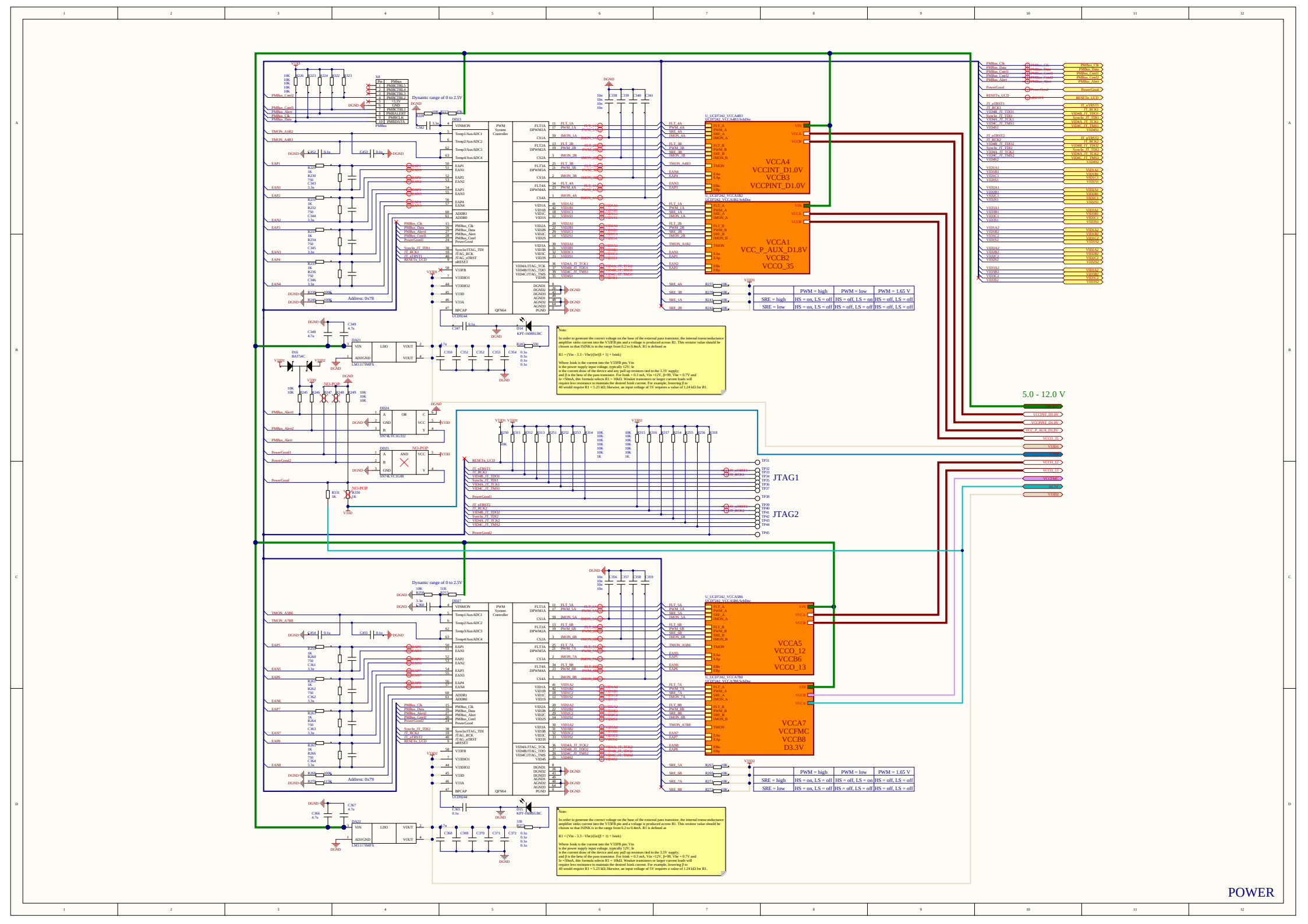
SI-XC7Z030-SOM-QTH

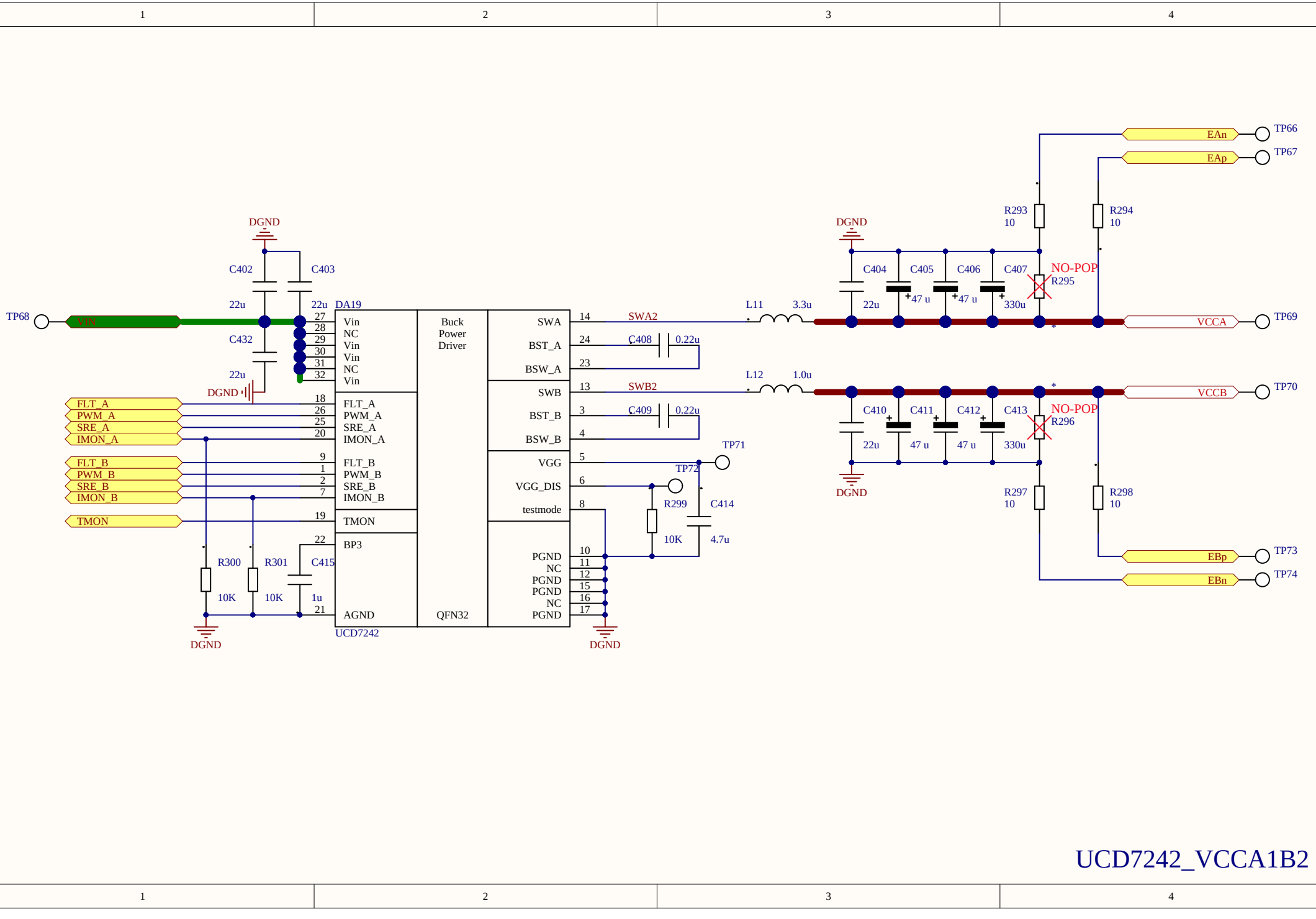




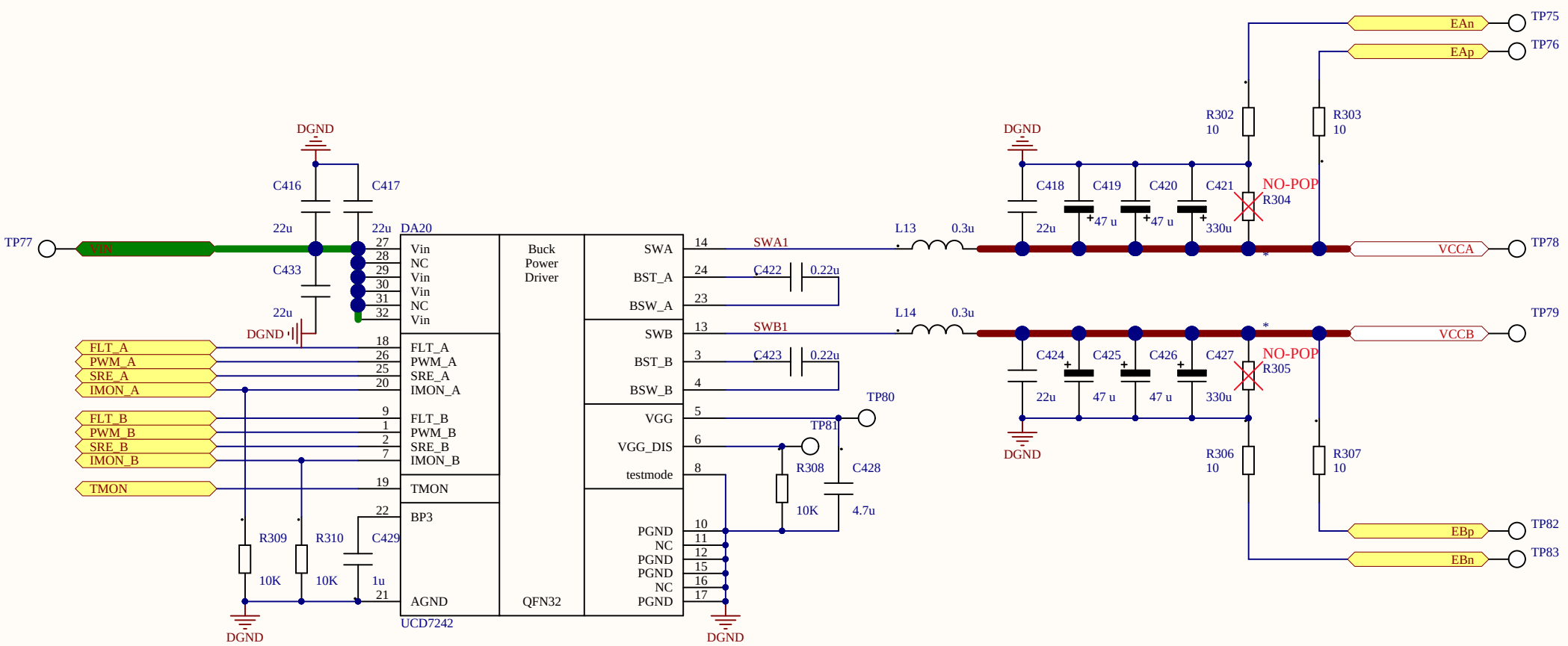
Processing System (PS)		Type V	Type A
VCCPINT	PS primary logic supply	1.00 V	*
VCCPAUX	PS auxiliary supply voltage	1.80 V	*
VCCPLL	PS PLL supply	1.80 V	*
VCCO_DDR	PS DDR I/O supply	1.35 V	*
VCCO_MIO	PS MIO I/O supply	3.3 V	*
VPREF	PS input reference voltage	1.25 V	*
Programmable Logic (PL)			
VCCINT	PL internal supply voltage	1.00 V	*
VCCAUX	PL auxiliary supply voltage	1.80 V	*
VCCBRAM	PL supply voltage for the block RAM memories	1.00 V	*
VCCO	PL output drivers supply voltage for 3.3V HR I/O banks PL output drivers supply voltage for 1.8V HP I/O banks	3.3 V	*
VCCAUX_IO	PS primary logic supply	2.00 V	42 mA
VREF	Input reference voltage	1.25 V	
VCCBATT	Battery voltage	1.8 V	150 nA

GTX Transceiver		Type V	Type A
VMGTAVCC	Analog supply voltage for the GTX transmitter and receiver circuits	1.00 V	
VMGTAVTT	Analog supply voltage for the GTX transmitter and receiver termination circuits	1.20 V	
VMGTVCCAUX	Auxiliary analog Quad PLL (QPLL) voltage supply for the GTX transceivers	1.80 V	
VMGTREFCLK	GTX transceiver reference clock absolute input voltage	2.00 V	
XADC			
VCCADC	XADC supply relative to GNDADC	1.8 V	25 mA
VREFP	XADC reference input relative to GNDADC	1.25 V	

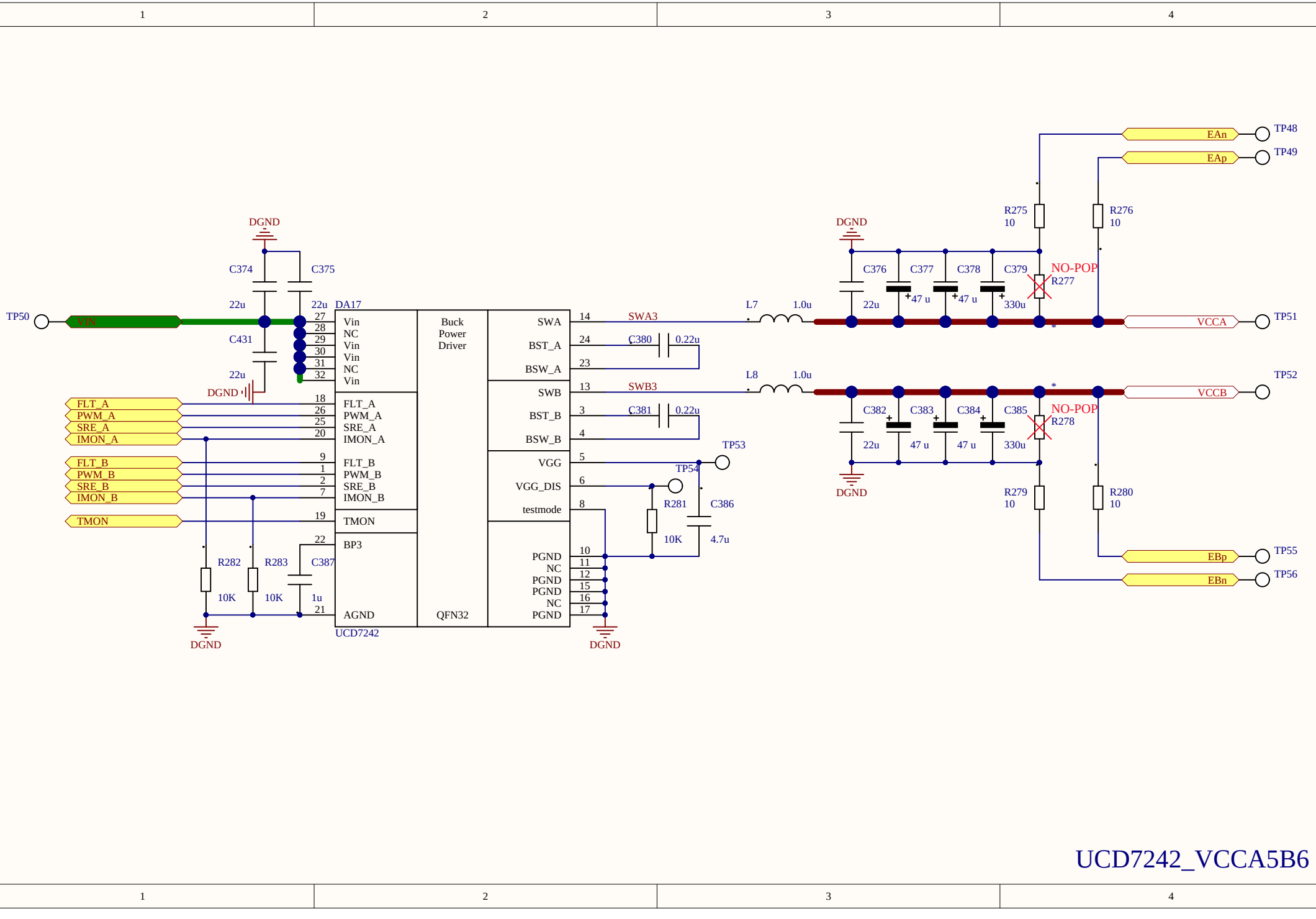

VCCA4
VCCINT_D1.0V
VCCB3
VCCPINT_D1.0V
VCCA1
VCC_P_AUX_D1.8V
VCCB2
VCCO_35
VCCA5
VCCO_12
VCCB6
VCCO_13
VCCA7
VCCFMC
VCCB8
D3.3V
JTAG1
JTAG2
5.0 - 12.0 V
Dynamic range of 0 to 2.5V
Address: 0x78
Address: 0x79
PWM = high
PWM = low
PWM = 1.65 V
SRE = high
SRE = low
HS = on, LS = off
HS = off, LS = on
HS = off, LS = off
POWER

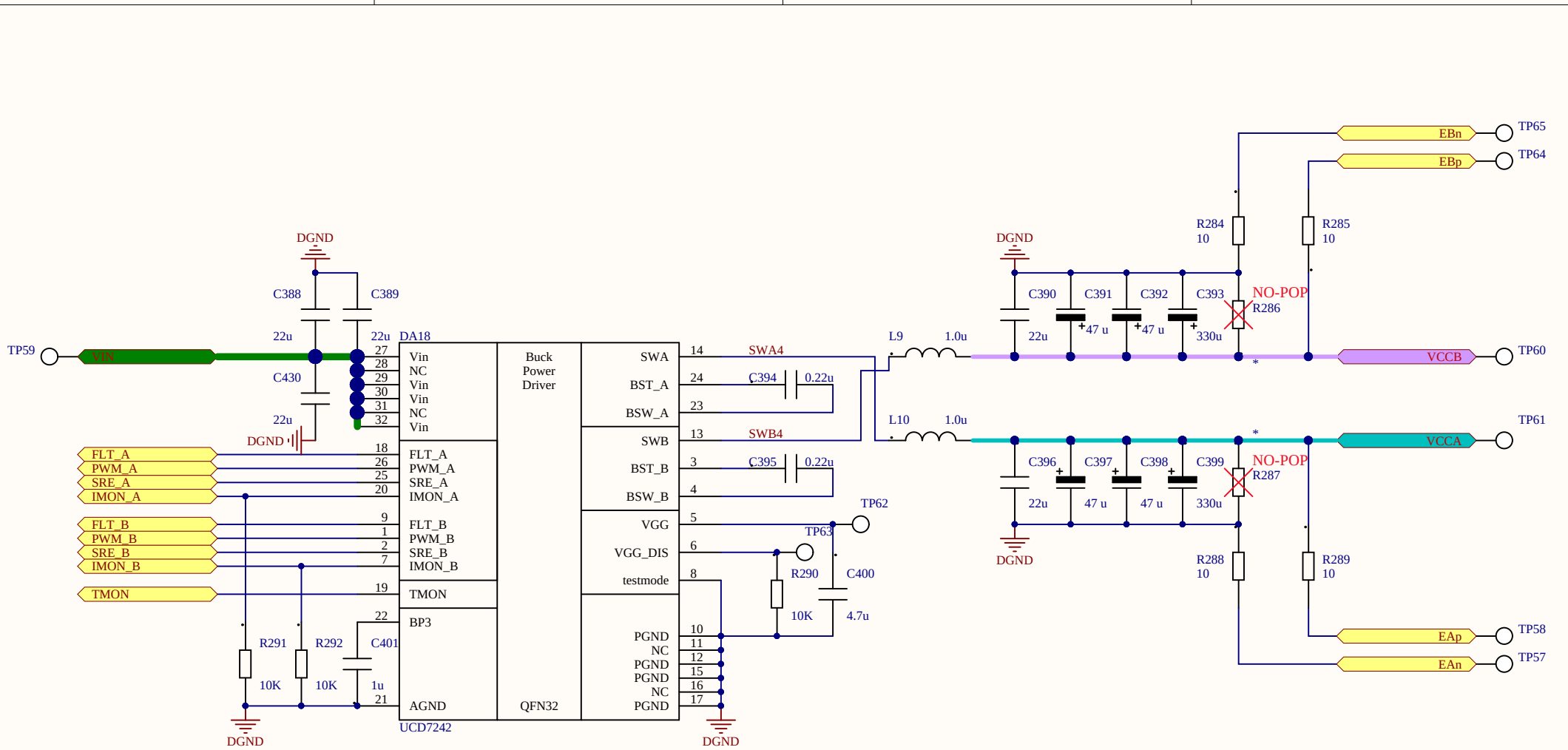


UCD7242_VCCA1B2

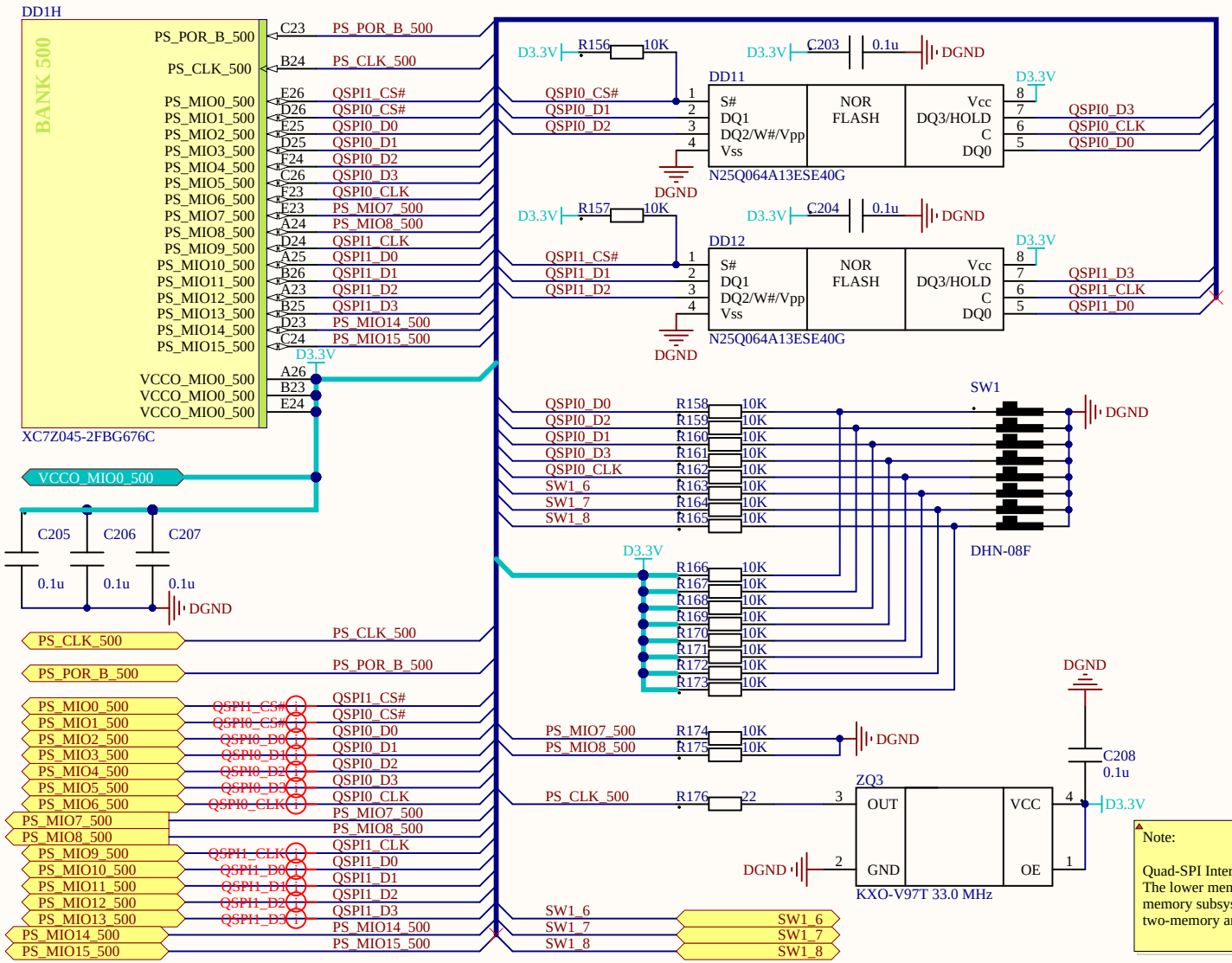


UCD7242_VCCA4B3


DA17
UCD7242
Buck
Power
Driver
QFN32
Vin
NC
Vin
Vin
NC
Vin
FLT_A
PWM_A
SRE_A
IMON_A
FLT_B
PWM_B
SRE_B
IMON_B
TMON
BP3
AGND
SWA
BST_A
BSW_A
SWB
BST_B
BSW_B
VGG
VGG_DIS
testmode
PGND
NC
PGND
PGND
NC
PGND
TP50
VIN
C374
C375
C431
22u
DGND
SWA3
SWB3
L7
L8
1.0u
C380
C381
0.22u
TP53
TP54
R281
10K
C386
4.7u
R282
R283
C387
1u
C376
C377
C378
C379
47 u
330u
NO-POP
R277
R278
R275
R276
R279
R280
10
EAn
EAp
TP48
TP49
VCCA
VCCB
TP51
TP52
EBp
EBn
TP55
TP56
UCD7242_VCCA5B6



UCD7242_VCCA7B8



Boot Mode MIO Strapping Pins

Mode	JTAG_C	JTAG_I	NOR	QSPI
MIO[2]	0	1	X	X
MIO[3]	0	0	1	0
MIO[4]	0	0	0	0
MIO[5]	0	0	0	1
MIO[6]	X	X	X	X
MIO[7]	X	X	X	X
MIO[8]	X	X	X	X

Mode	SDCard	PLL_En	PLL_By
MIO[2]	X	X	X
MIO[3]	0	X	X
MIO[4]	1	X	X
MIO[5]	1	X	X
MIO[6]	X	0	1
MIO[7]	X	X	X
MIO[8]	X	X	X

Mode	Bank01 = 2.5V, 3.3V	Bank01 = 1.8V
MIO[2]	X	X
MIO[3]	X	X
MIO[4]	X	X
MIO[5]	X	X
MIO[6]	X	X
MIO[7]	0	1
MIO[8]	0	1

Note:

Quad-SPI Interface:
The lower memory Quad-SPI interface (QSPI_0) must be used if the Quad-SPI memory subsystem is to be used. The upper interface (QSPI_1) is optional and is only used for a two-memory arrangement (parallel or stacked). Do not use the Quad-SPI 1 interface alone.

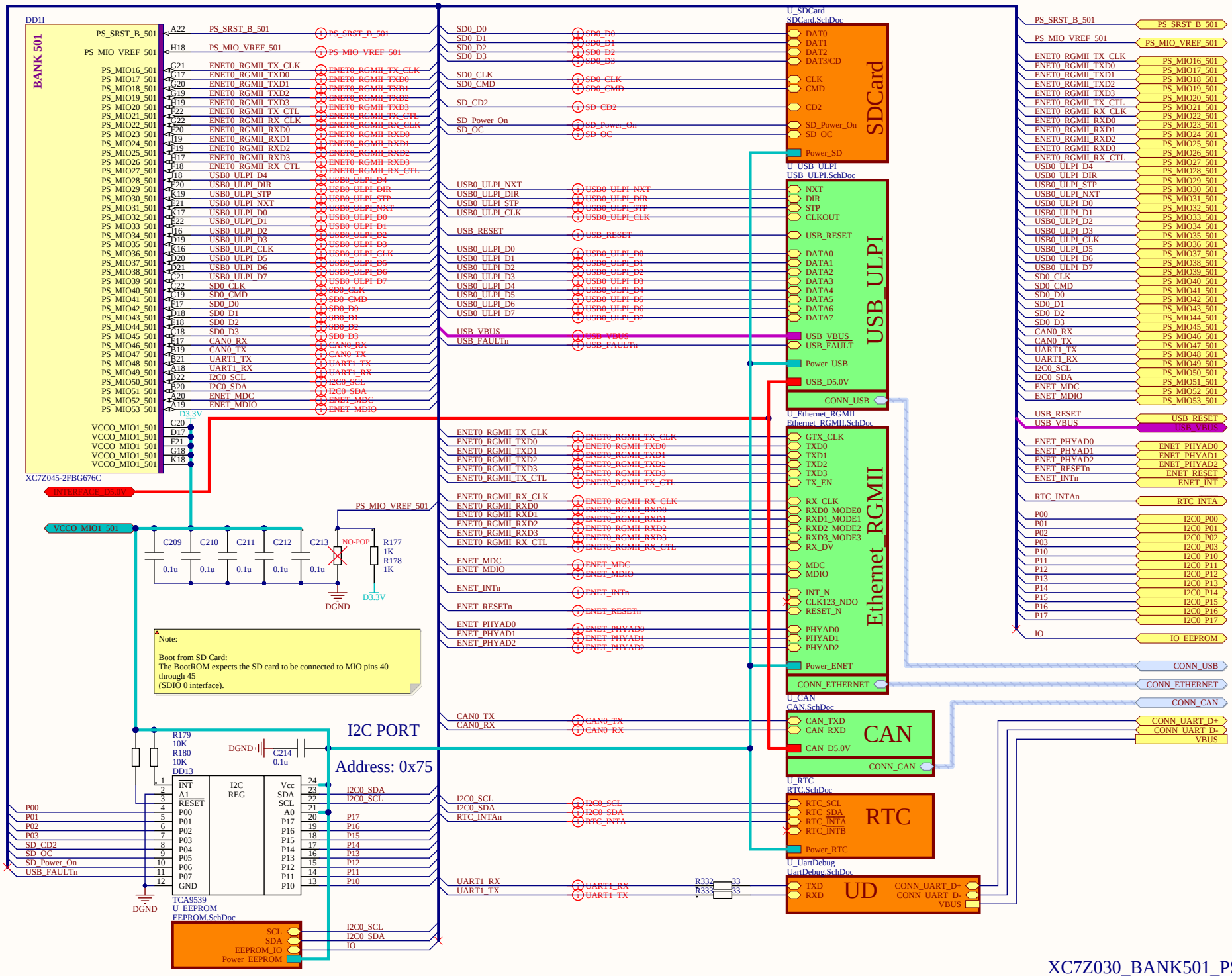
Note:

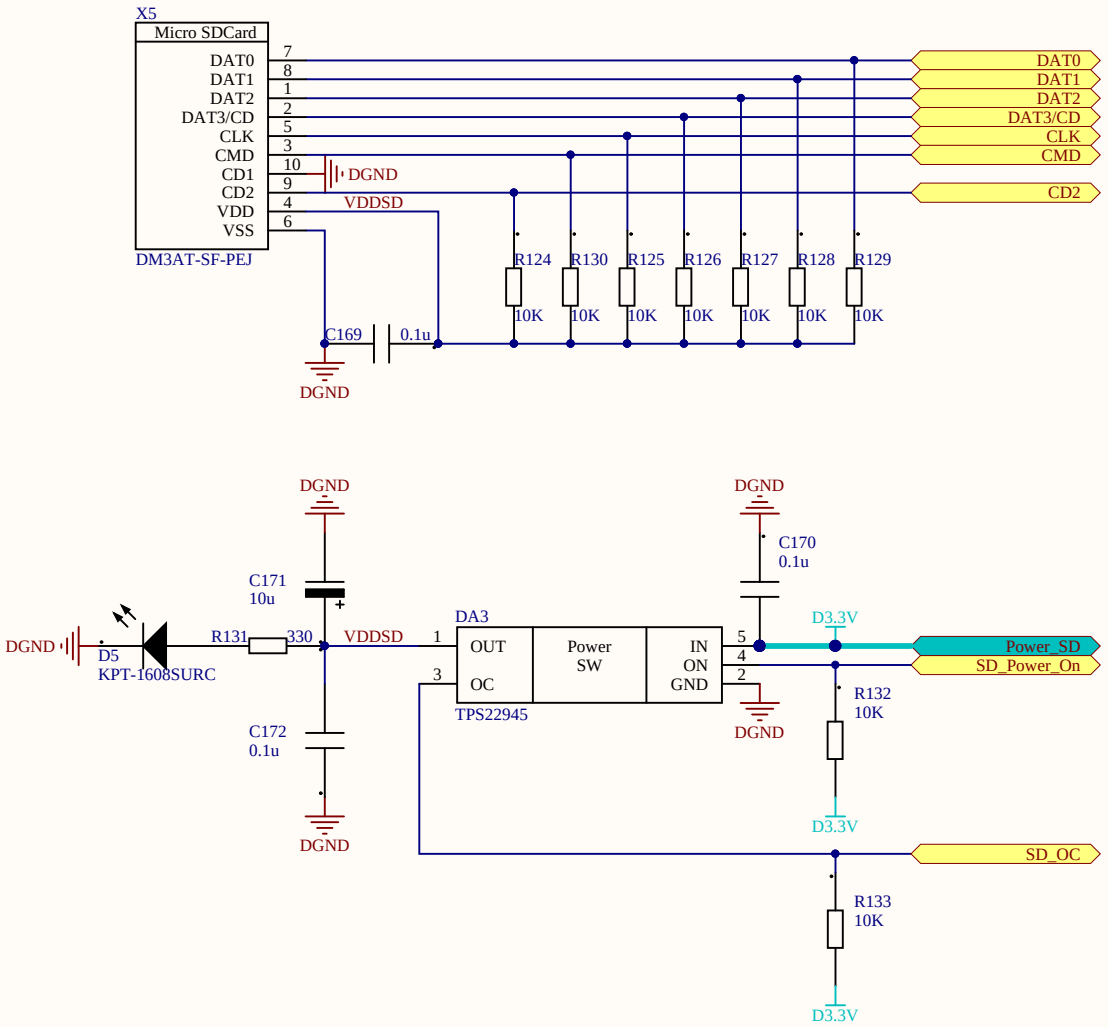
MIO Pins [8:7] are Outputs:
These MIO pins are available as output only. GPIO channels 7 and 8 can only be configured as outputs

Note:

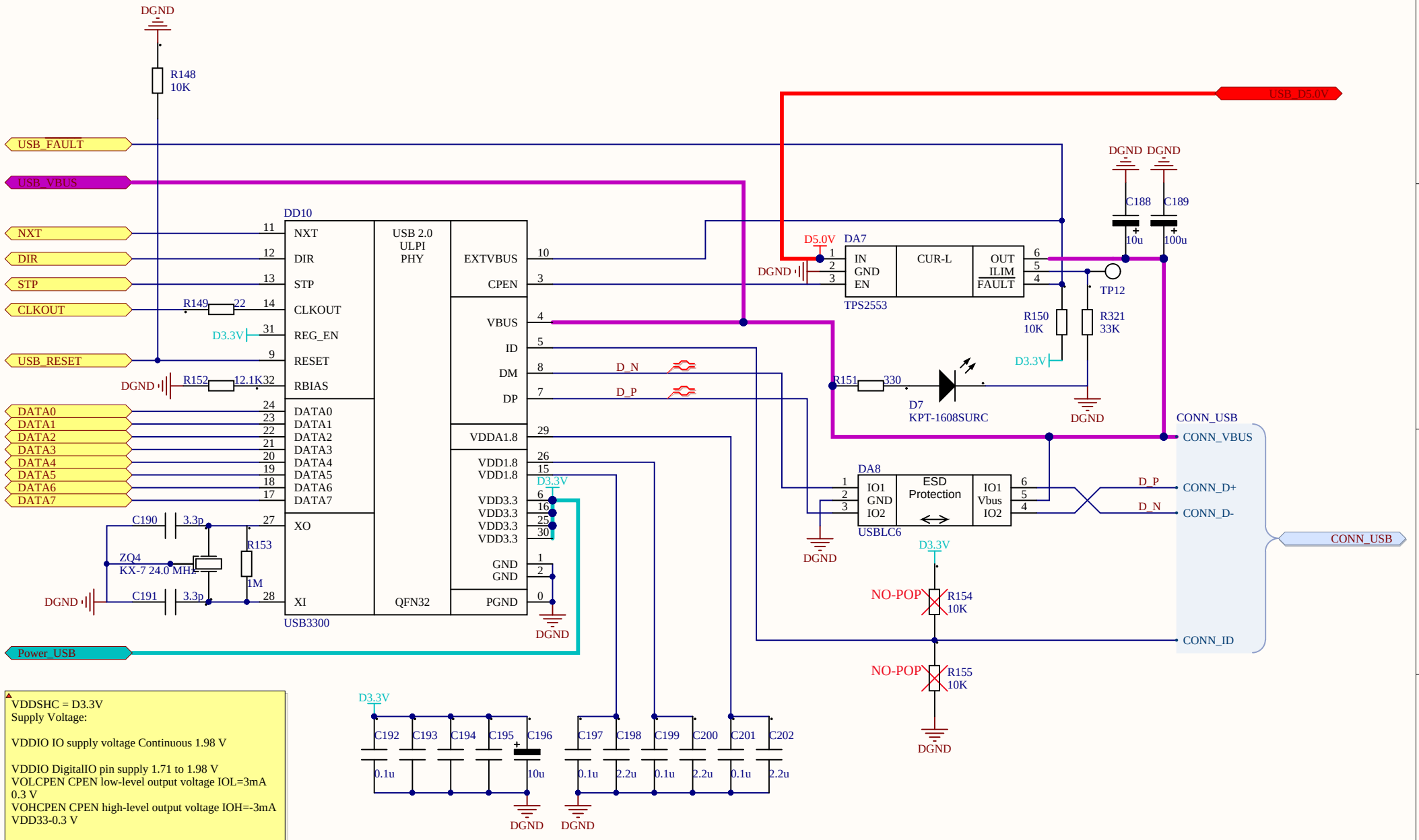
Boot Mode Strapping Pins:
These pins can be assigned to I/O peripherals in addition to functioning as boot mode pins. MIO pins [8:2], define the bootdevice, the initial PLL clock bypass mode, and the voltage mode (VMODE) for the MIO banks. The strapping pins are sampled a few PS_CLK clock cycles after the PS_POR_B reset signal de-asserts. The board design ties these signals to VCC or ground using 20 K?pull-up and pull-down resisters. More information about the boot mode pin settings is provided in Chapter 6, Boot and Configuration.

XC7Z030_BANK500_PS_QSPI-FL_BOOT


DD1I
BANK 501
XC7Z045-2FBG676C
U_SDCard
SDCard.SchDoc
SDCard
U_USB_ULPI
USB_ULPI.SchDoc
USB_ULPI
U_Ethernet_RGMII
Ethernet_RGMII.SchDoc
Ethernet_RGMII
U_CAN
CAN.SchDoc
CAN
U_RTC
RTC.SchDoc
RTC
U_UartDebug
UartDebug.SchDoc
UD
INTERFACE_D5.0V
D3.3V
VCCO_MIO1_501
PS_MIO_VREF_501
DGND
NO-POP
R177
1K
R178
1K
C209
C210
C211
C212
C213
0.1u
Note:
Boot from SD Card:
The BootROM expects the SD card to be connected to MIO pins 40 through 45
(SDIO 0 interface).
I2C PORT
Address: 0x75
R179
10K
R180
10K
C214
0.1u
DD13
TCA9539
U_EEPROM
EEPROM.SchDoc
CONN_USB
CONN_ETHERNET
CONN_CAN
CONN_UART_D+
CONN_UART_D-
VBUS
IO_EEPROM
XC7Z030_BANK501_PS_INTERFACE


X5
Micro SDCard
DAT0
DAT1
DAT2
DAT3/CD
CLK
CMD
CD1
CD2
VDD
VSS
7
8
1
2
5
3
10
9
4
6
DM3AT-SF-PEJ
DGND
VDDSD
DAT0
DAT1
DAT2
DAT3/CD
CLK
CMD
CD2
R124
R130
R125
R126
R127
R128
R129
10K
C169
0.1u
DGND
DGND
C171
10u
DGND
R131
330
D5
KPT-1608SURC
VDDSD
DA3
OUT
OC
Power
SW
IN
ON
GND
1
3
5
4
2
TPS22945
DGND
C170
0.1u
D3.3V
Power_SD
SD_Power_On
R132
10K
D3.3V
C172
0.1u
DGND
SD_OC
R133
10K
D3.3V

SDCard


DGND
R148
10K
USB_FAULT
USB_VBUS
USB_D5.0V
NXT
DIR
STP
CLKOUT
USB_RESET
DATA0
DATA1
DATA2
DATA3
DATA4
DATA5
DATA6
DATA7
DD10
USB 2.0
ULPI
PHY
QFN32
USB3300
R149
22
D3.3V
R152
12.1K
C190
3.3p
ZQ4
KX-7 24.0 MHz
R153
1M
C191
3.3p
Power_USB
D5.0V
DA7
IN
GND
EN
CUR-L
OUT
ILIM
FAULT
TPS2553
C188
C189
10u
100u
TP12
R150
10K
R321
33K
R151
330
D7
KPT-1608SURC
DA8
IO1
GND
IO2
ESD
Protection
IO1
Vbus
IO2
USBLC6
CONN_USB
CONN_VBUS
CONN_D+
CONN_D-
CONN_ID
D_P
D_N
NO-POP
R154
10K
R155
10K
C192
C193
C194
C195
C196
C197
C198
C199
C200
C201
C202
0.1u
2.2u
VDDSHC = D3.3V
Supply Voltage:
VDDIO IO supply voltage Continuous 1.98 V
VDDIO DigitalIO pin supply 1.71 to 1.98 V
VOLCPEN CPEN low-level output voltage IOL=3mA
0.3 V
VOHCPEN CPEN high-level output voltage IOH=-3mA
VDD33-0.3 V
VOL Max 0.45 V
USB_ULPI

Single-LED Mode

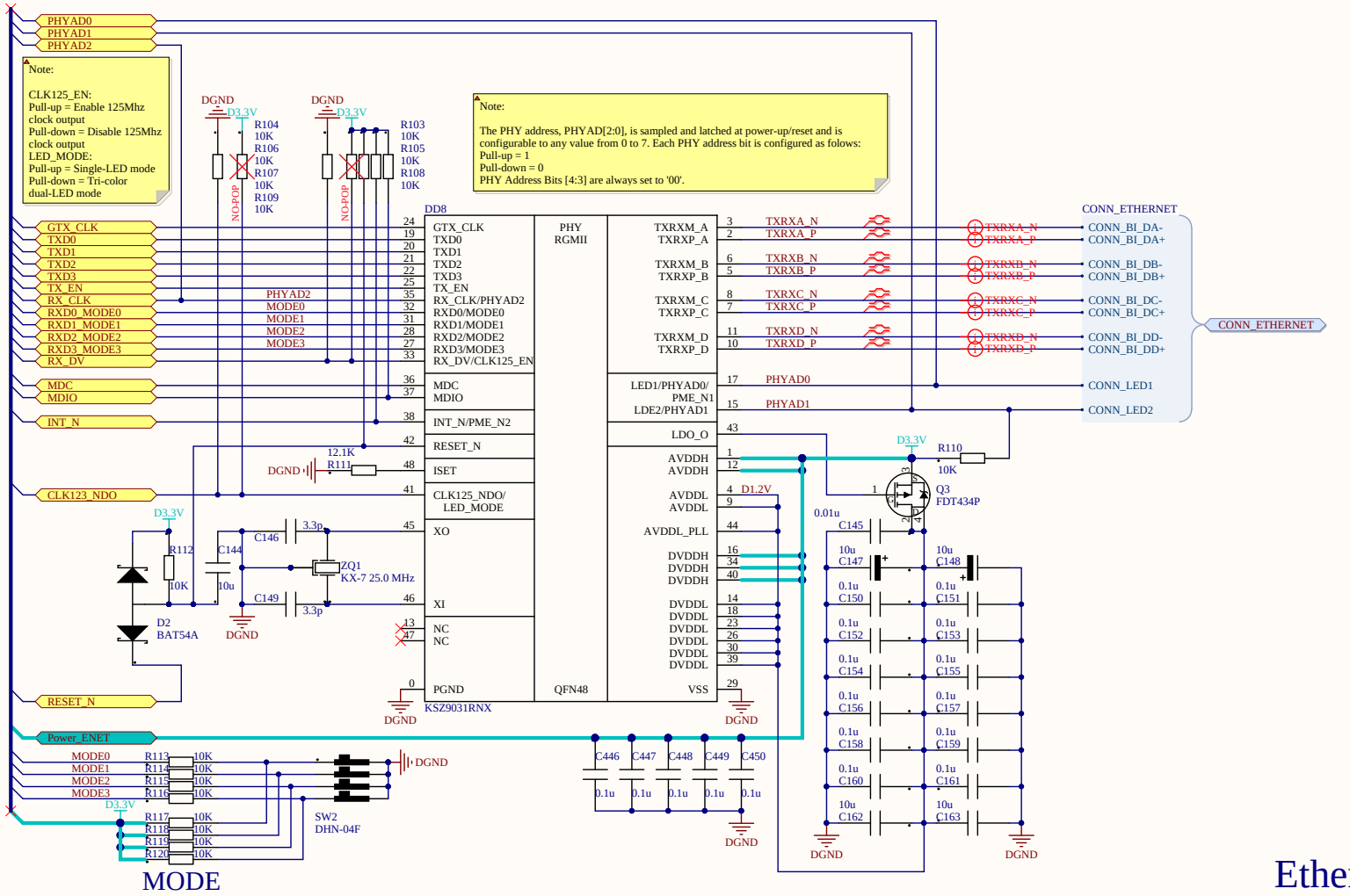
Link	Pin State	LED Definition
Link off	H	OFF
Link on	L	ON

Tri-Color Dual-LED Mode

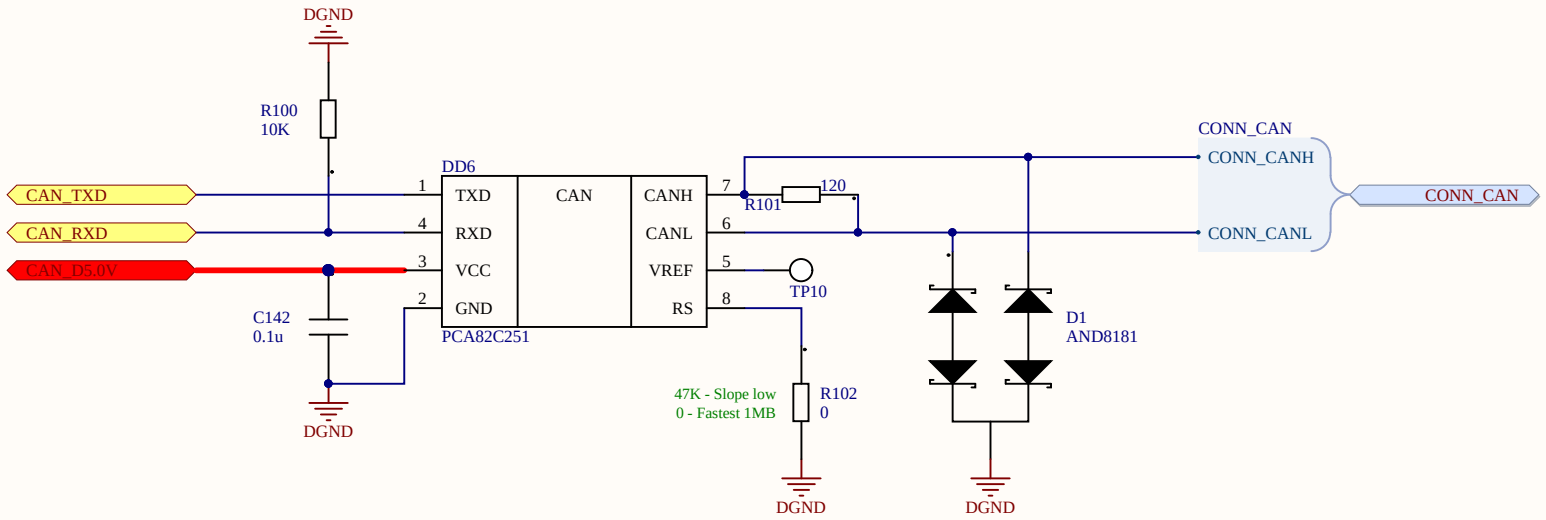
Link/Activity	Pin State		LED Definition	
	LED2	LED1	LED2	LED1
Link off	H	H	OFF	OFF
1000 Link / No activity	L	H	ON	OFF
1000 Link / Activity (RX, TX)	Toggle	H	Blinking	OFF
100 Link / No activity	H	L	OFF	ON
100 Link / Activity (RX, TX)	H	Toogle	OFF	Blinking
10 Link / No activity	L	L	ON	ON
10 Link / Activity (RX, TX)	Toogle	Toogle	Blinking	Blinking

Strapping Pins

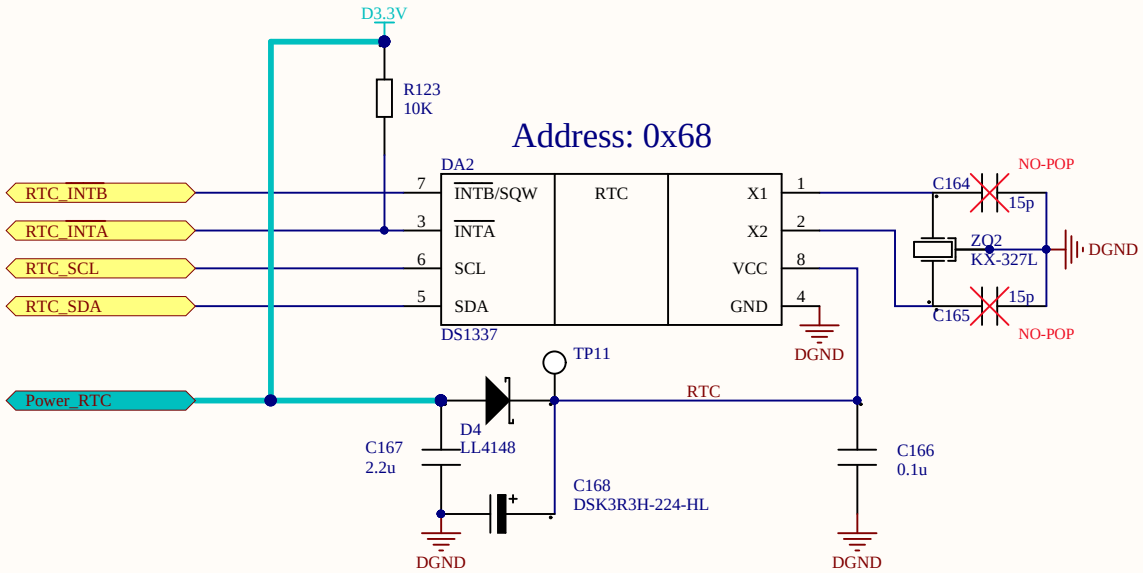
MODE[3:0]	MODE
0100	NAND tree mode
0111	Chip power-down mode
1100	RGMII mode - advertise 1000Base-T full-duplex only
1101	RGMII mode - advertise 1000Base-T full- and half-duplex onlyduplex only
1110	RGMII mode - advertise all capabilities (10/100/1000 speed half-/full-duplex), except 1000Base-T half-duplex
1111	RGMII mode - advertise all capabilities (10/100/1000 speed half-/full-duplex)



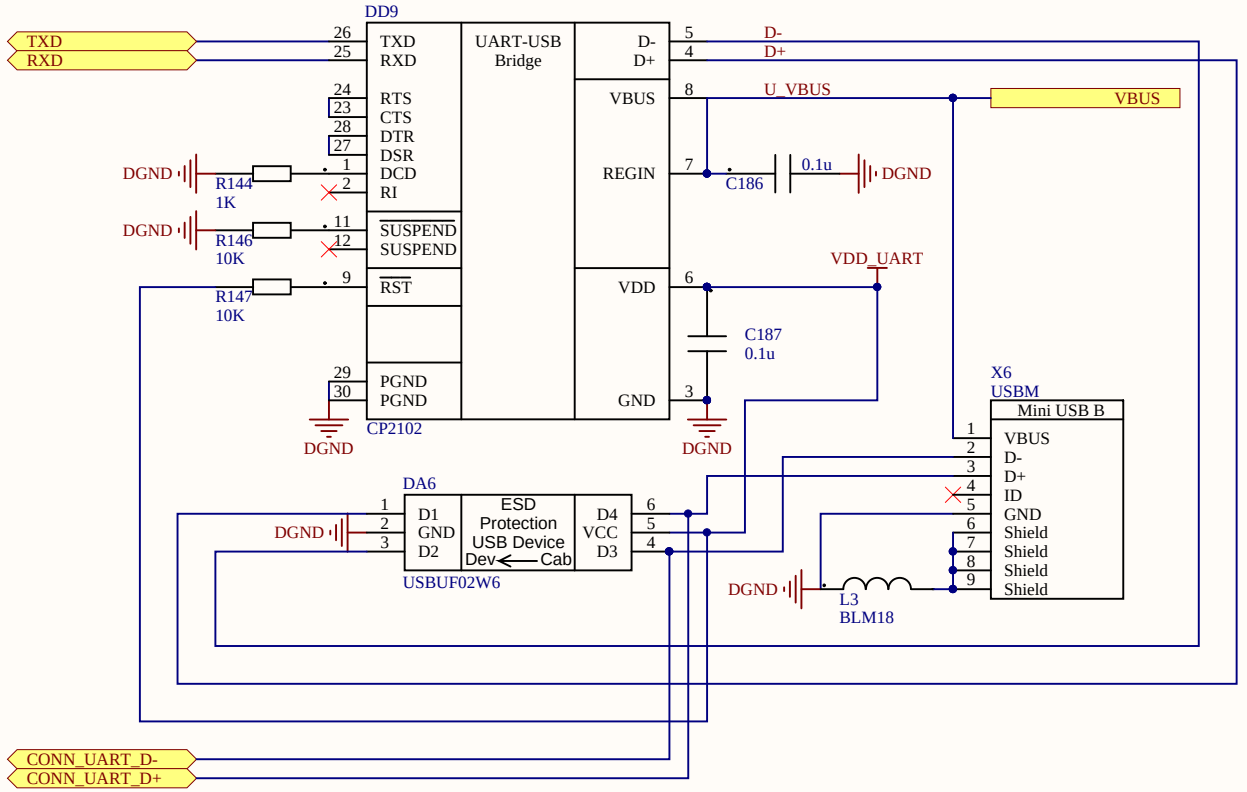
Ethernet_RGMII


DGND
R100
10K
CAN_TXD
CAN_RXD
CAN_D5.0V
C142
0.1u
DGND
DD6
1
4
3
2
TXD
RXD
VCC
GND
CAN
CANH
CANL
VREF
RS
7
6
5
8
PCA82C251
R101
120
TP10
47K - Slope low
0 - Fastest 1MB
R102
0
DGND
D1
AND8181
DGND
CONN_CAN
CONN_CANH
CONN_CANL
CONN_CAN

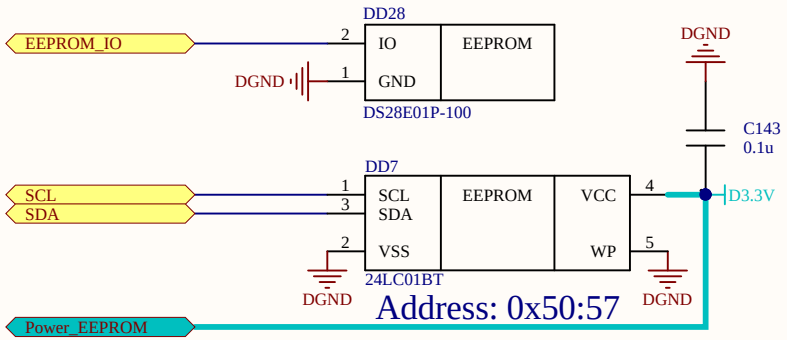
CAN


D3.3V
R123
10K
Address: 0x68
DA2
RTC_INTB
RTC_INTA
RTC_SCL
RTC_SDA
7
3
6
5
INTB/SQW
INTA
SCL
SDA
RTC
X1
X2
VCC
GND
1
2
8
4
DS1337
DGND
NO-POP
C164
15p
ZQ2
KX-327L
DGND
C165
15p
NO-POP
TP11
Power_RTC
RTC
D4
LL4148
C167
2.2u
C168
DSK3R3H-224-HL
C166
0.1u
DGND
DGND

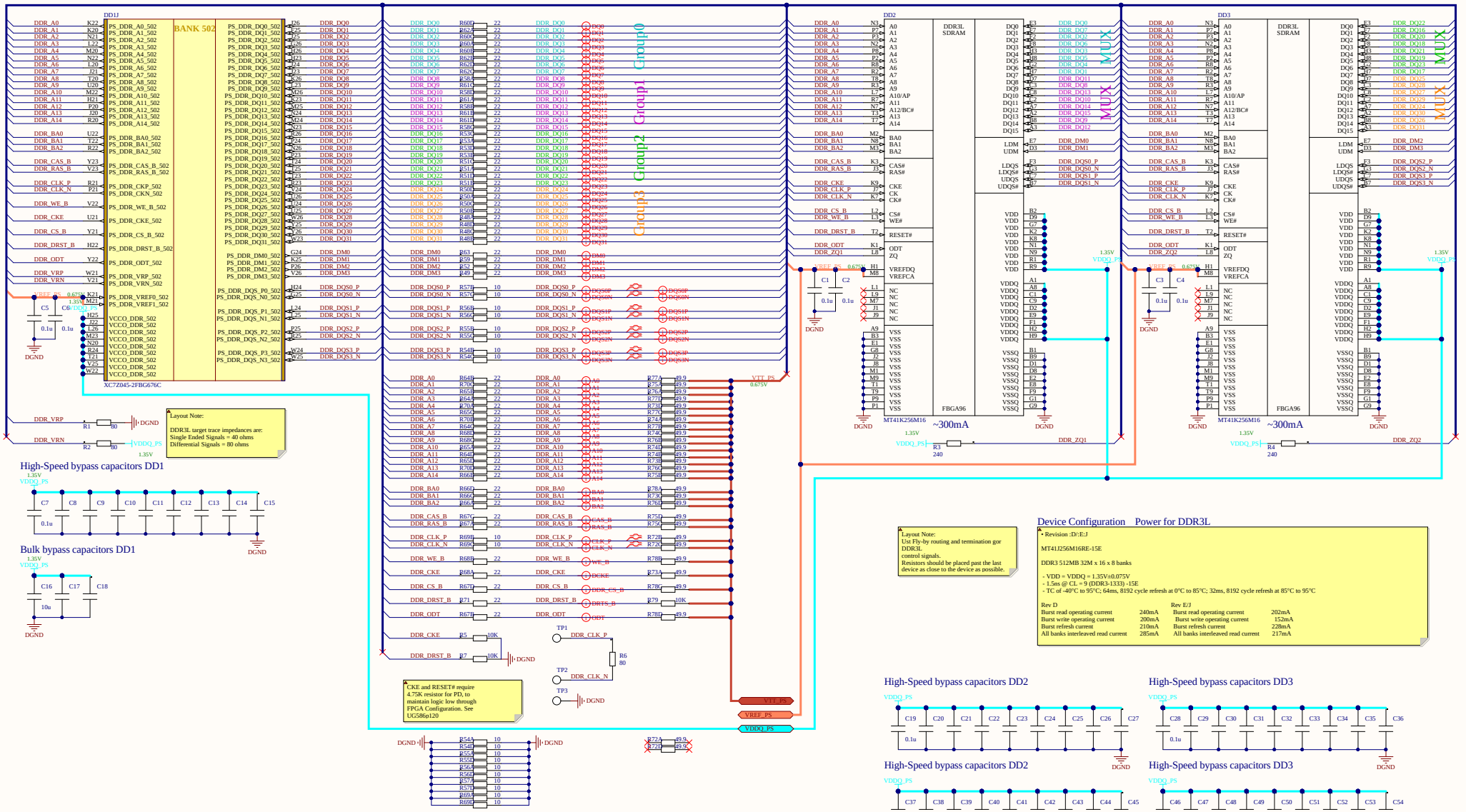
RTC


DD9
TXD
RXD
26
25
TXD
RXD
UART-USB
Bridge
D-
D+
5
4
D-
D+
24
23
28
27
RTS
CTS
DTR
DSR
VBUS
8
U_VBUS
VBUS
DGND
R144
1K
1
2
DCD
RI
REGIN
7
C186
0.1u
DGND
DGND
R146
10K
11
12
SUSPEND
SUSPEND
VDD_UART
R147
10K
9
RST
VDD
6
C187
0.1u
29
30
PGND
PGND
GND
3
X6
USBM
Mini USB B
DGND
DGND
CP2102
DA6
1
2
3
D1
GND
D2
ESD
Protection
USB Device
Dev
Cab
D4
VCC
D3
6
5
4
USBUF02W6
VBUS
D-
D+
ID
GND
Shield
Shield
Shield
Shield
DGND
L3
BLM18
CONN_UART_D-
CONN_UART_D+

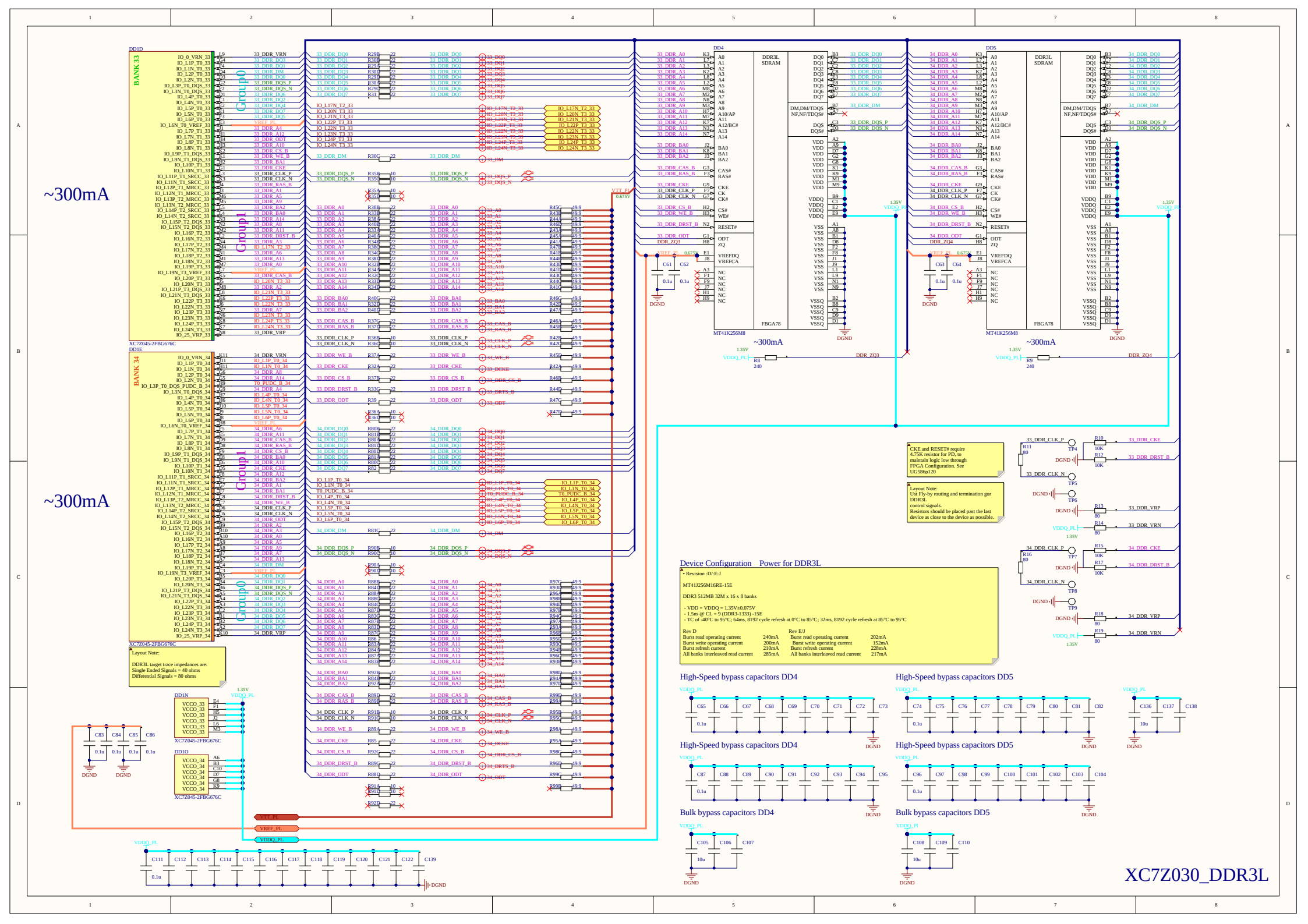
UartDebug

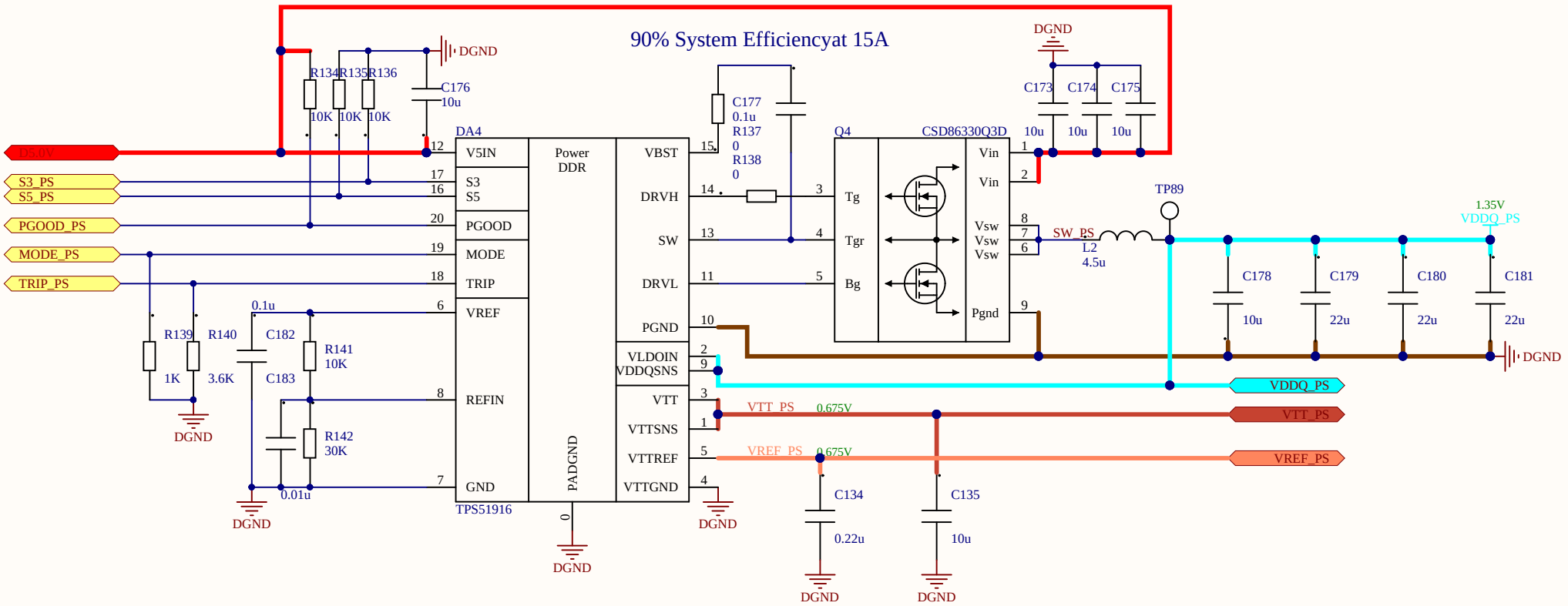

DD28
EEPROM_IO
2
IO
EEPROM
DGND
1
GND
DS28E01P-100
DGND
C143
0.1u
DD7
SCL
SDA
1
3
SCL
SDA
EEPROM
VCC
4
D3.3V
2
VSS
WP
5
24LC01BT
DGND
DGND
Address: 0x50:57
Power_EEPROM

EEPROM



XC7Z030_PS_DDR3L


~300mA
~300mA
~300mA
~300mA
DD1D
BANK 33
XC7Z045-2FBG676C
DD1E
BANK 34
XC7Z045-2FBG676C
Group0
Group1
Group1
Group0
DD4
DDR3L SDRAM
FBGA78
MT41K256M8
DD5
DDR3L SDRAM
FBGA78
MT41K256M8
CKE and RESET# require 4.75K resistor for PD, to maintain logic low through FPGA Configuration. See UG586p120
Layout Note: Use Fly-by routing and termination gor DDR3L control signals. Resistors should be placed past the last device as close to the device as possible.
Layout Note: DDR3L target trace impedances are: Single Ended Signals = 40 ohms Differential Signals = 80 ohms
Device Configuration Power for DDR3L
• Revision :D/E/J
MT41J256M16RE-15E
DDR3 512MB 32M x 16 x 8 banks
- VDD = VDDQ = 1.35V±0.075V
- 1.5ns @ CL = 9 (DDR3-1333) -15E
- TC of -40°C to 95°C; 64ms, 8192 cycle refresh at 0°C to 85°C; 32ms, 8192 cycle refresh at 85°C to 95°C
Rev D
Burst read operating current 240mA
Burst write operating current 200mA
Burst refresh current 210mA
All banks interleaved read current 285mA
Rev E/J
Burst read operating current 202mA
Burst write operating current 152mA
Burst refresh current 228mA
All banks interleaved read current 217mA
High-Speed bypass capacitors DD4
High-Speed bypass capacitors DD5
High-Speed bypass capacitors DD4
High-Speed bypass capacitors DD5
Bulk bypass capacitors DD4
Bulk bypass capacitors DD5
XC7Z030_DDR3L



Device Configuration for DDR3/3L

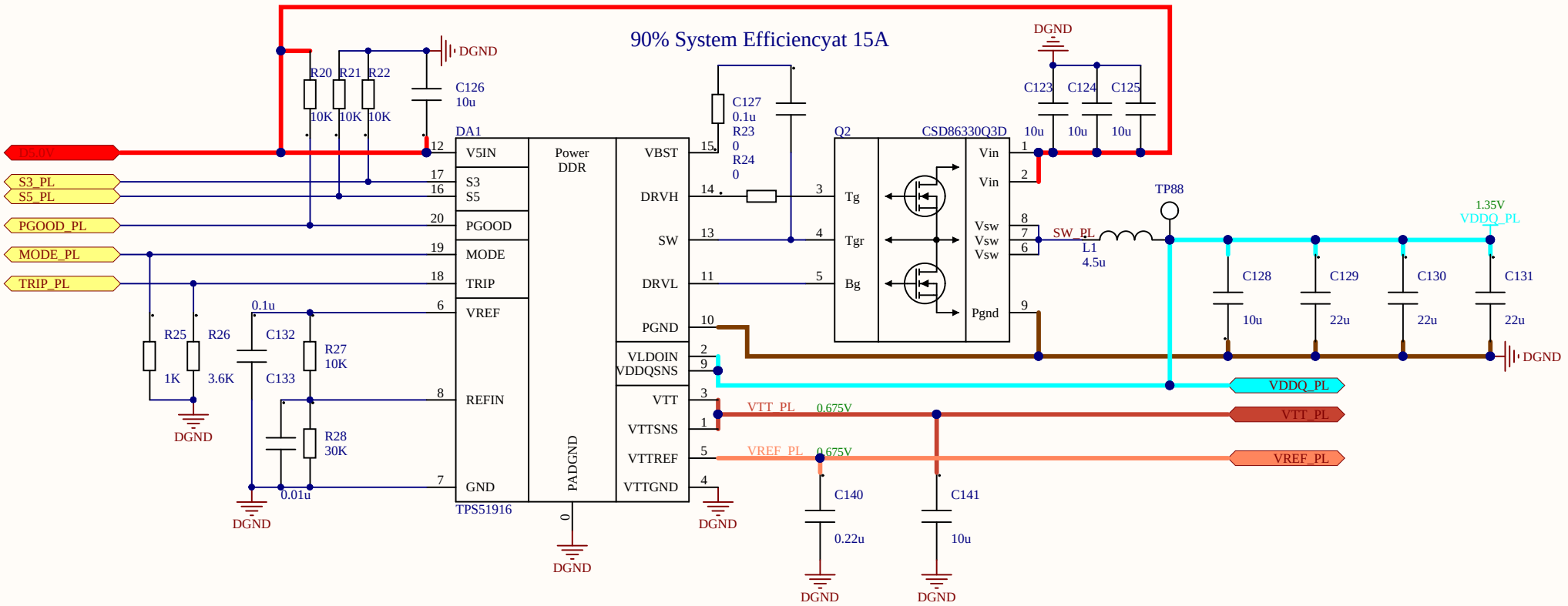
MODE: R = 1K Fsw = 500KHz
TRIP: CDS86350Q5D Rds = 2mO Iocl = 2.5A Rtrip = 3.6K

Vin = 5.5V VDDQ = 1.35V VTT = 0.675V

Iout = 1.8A Iind(ripple) = 0.6A Iind(peak) = 2.75A Ivtt = 1.2A

Cout > 57u

TPS51916_PW_DDR3L_PS



Device Configuration for DDR3/3L

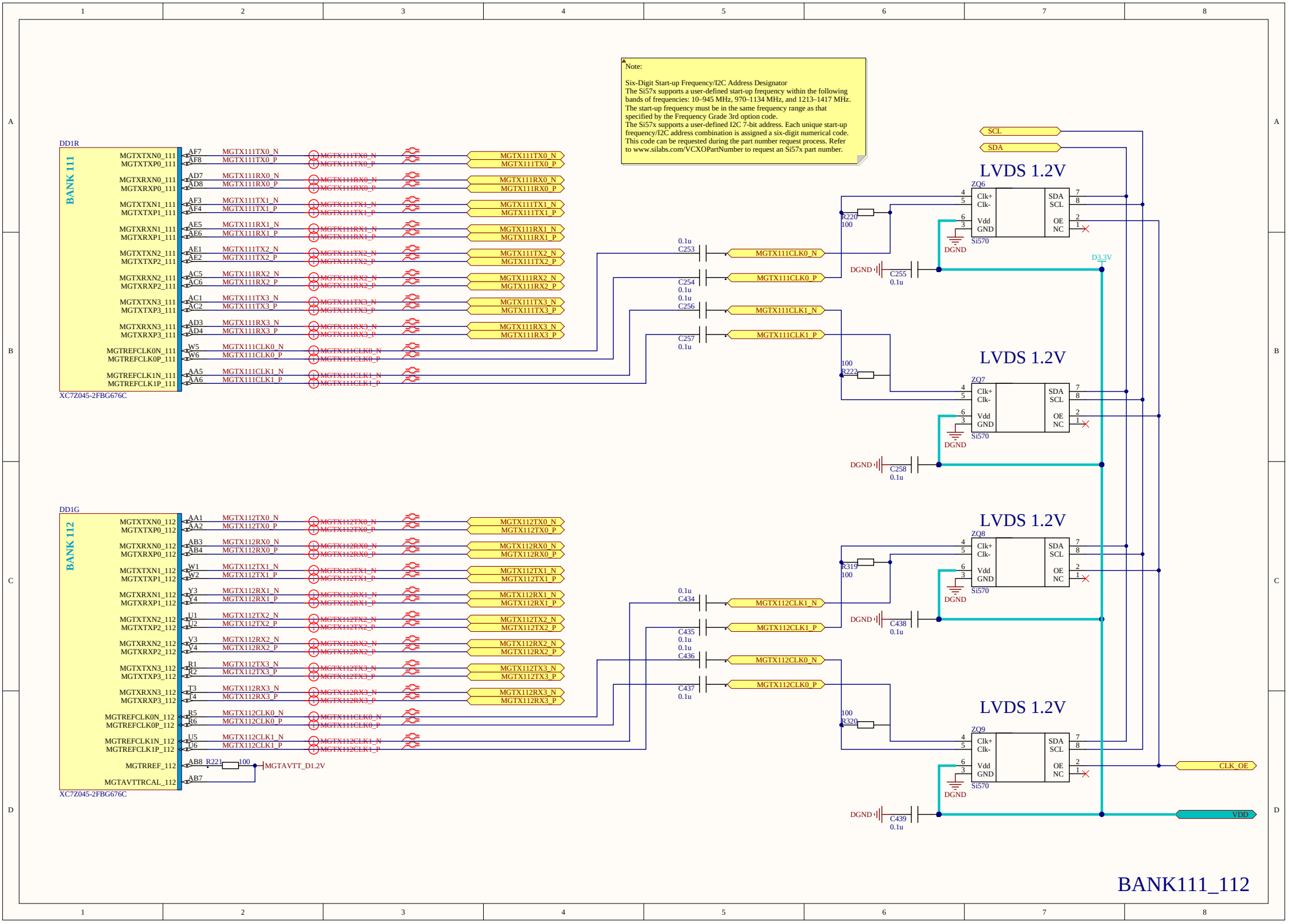
MODE: R = 1K Fsw = 500KHz
TRIP: CDS86350Q5D Rds = 2mO Iocl = 2.5A Rtrip = 3.6K

Vin = 5.5V VDDQ = 1.35V VTT = 0.675V

Iout = 1.8A Iind(ripple) = 0.6A Iind(peak) = 2.75A Ivtt = 1.2A

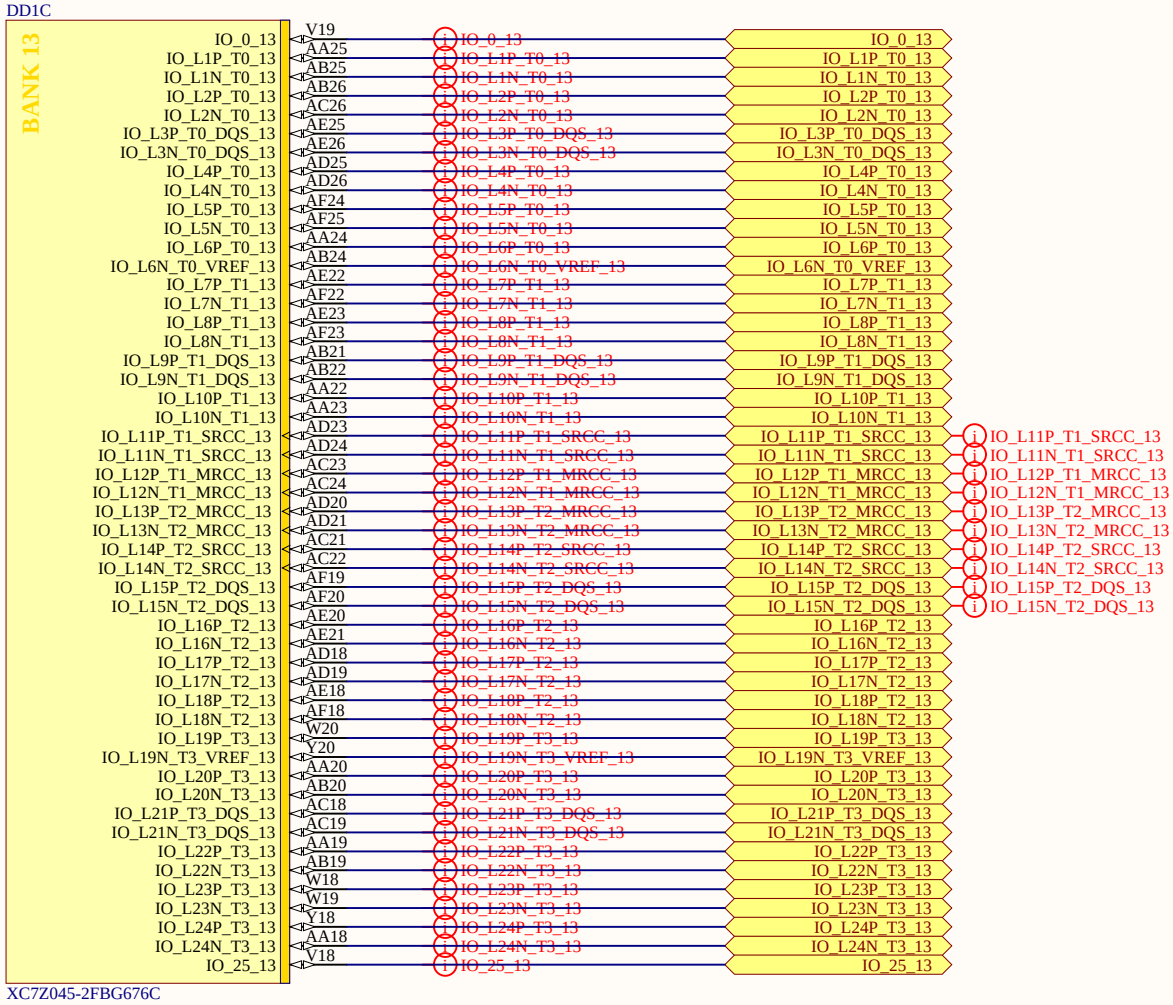
Cout > 57u

TPS51916_PW_DDR3L_PL

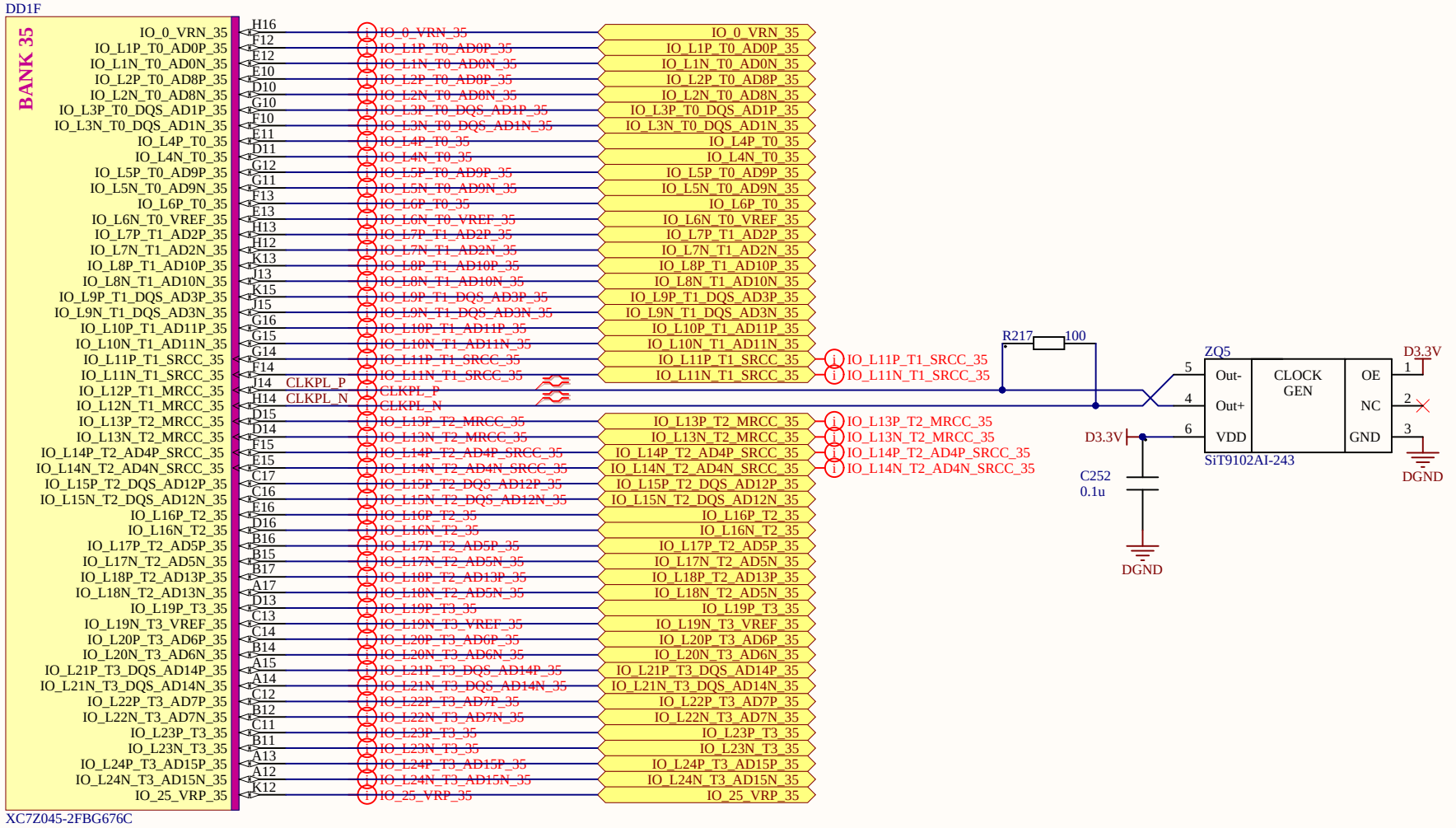

Note:
Six-Digit Start-up Frequency/I2C Address Designator
The Si57x supports a user-defined start-up frequency within the following bands of frequencies: 10–945 MHz, 970–1134 MHz, and 1213–1417 MHz. The start-up frequency must be in the same frequency range as that specified by the Frequency Grade 3rd option code.
The Si57x supports a user-defined I2C 7-bit address. Each unique start-up frequency/I2C address combination is assigned a six-digit numerical code. This code can be requested during the part number request process. Refer to www.silabs.com/VCXOPartNumber to request an Si57x part number.
DD1R
BANK 111
XC7Z045-2FBG676C
DD1G
BANK 112
XC7Z045-2FBG676C
LVDS 1.2V
LVDS 1.2V
LVDS 1.2V
LVDS 1.2V
ZQ6
ZQ7
ZQ8
ZQ9
Si570
SCL
SDA
CLK_OE
VDD
D3.3V
DGND
MGTAVTT_D1.2V
BANK111_112

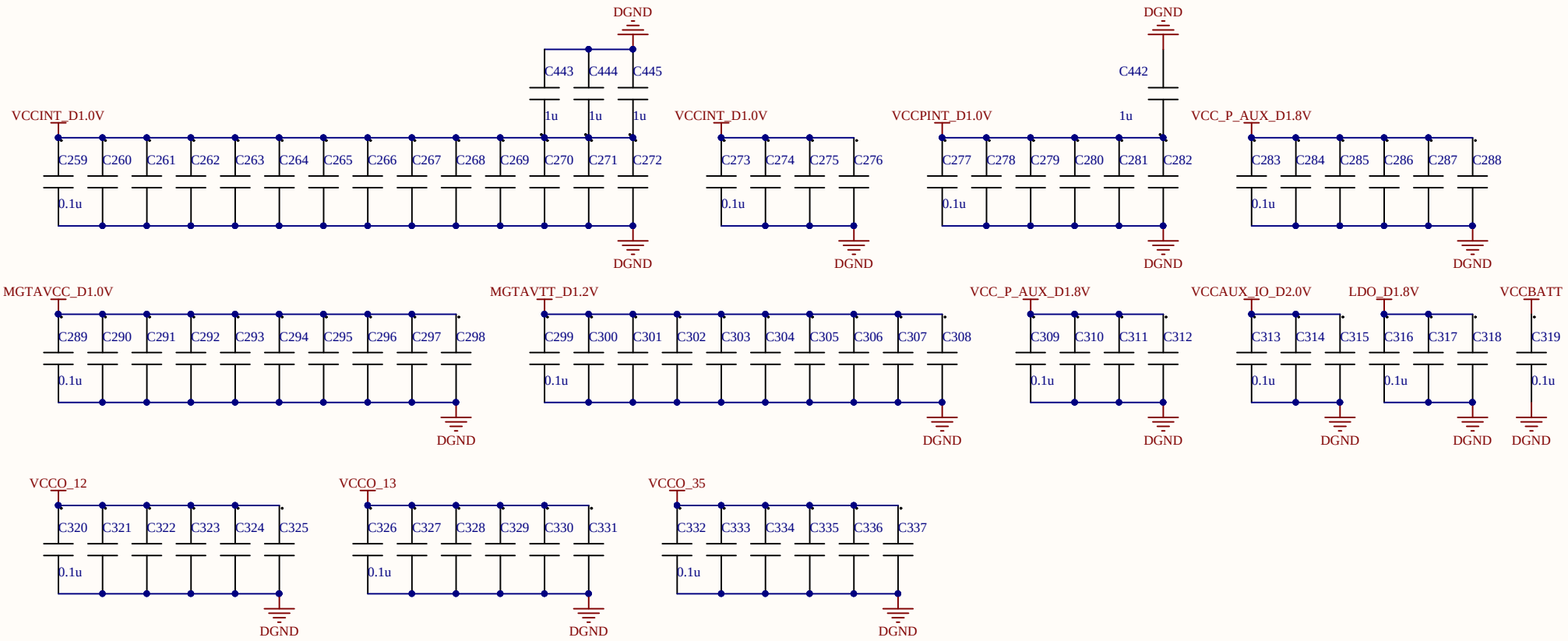

DD1B
BANK 12
IO_0_12
IO_L1P_T0_12
IO_L1N_T0_12
IO_L2P_T0_12
IO_L2N_T0_12
IO_L3P_T0_DQS_12
IO_L3N_T0_DQS_12
IO_L4P_T0_12
IO_L4N_T0_12
IO_L5P_T0_12
IO_L5N_T0_12
IO_L6P_T0_12
IO_L6N_T0_VREF_12
IO_L7P_T1_12
IO_L7N_T1_12
IO_L8P_T1_12
IO_L8N_T1_12
IO_L9P_T1_DQS_12
IO_L9N_T1_DQS_12
IO_L10P_T1_12
IO_L10N_T1_12
IO_L11P_T1_SRCC_12
IO_L11N_T1_SRCC_12
IO_L12P_T1_MRCC_12
IO_L12N_T1_MRCC_12
IO_L13P_T2_MRCC_12
IO_L13N_T2_MRCC_12
IO_L14P_T2_SRCC_12
IO_L14N_T2_SRCC_12
IO_L15P_T2_DQS_12
IO_L15N_T2_DQS_12
IO_L16P_T2_12
IO_L16N_T2_12
IO_L17P_T2_12
IO_L17N_T2_12
IO_L18P_T2_12
IO_L18N_T2_12
IO_L19P_T3_12
IO_L19N_T3_VREF_12
IO_L20P_T3_12
IO_L20N_T3_12
IO_L21P_T3_DQS_12
IO_L21N_T3_DQS_12
IO_L22P_T3_12
IO_L22N_T3_12
IO_L23P_T3_12
IO_L23N_T3_12
IO_L24P_T3_12
IO_L24N_T3_12
IO_25_12
W14
Y12
Y11
AB12
AC11
Y10
AA10
AB11
AB10
W13
Y13
AA13
AA12
AE10
AD10
AE12
AF12
AE11
AF10
AE13
AF13
AC12
AD11
AC13
AD13
AC14
AD14
AB15
AB14
AD16
AD15
AF15
AF14
AE16
AE15
AE17
AF17
Y17
AA17
AB17
AB16
AC17
AC16
AA15
AA14
Y16
Y15
W16
W15
W17
XC7Z045-2FBG676C

BANK12


DD1C
BANK 13
IO_0_13 V19
IO_L1P_T0_13 AA25
IO_L1N_T0_13 AB25
IO_L2P_T0_13 AB26
IO_L2N_T0_13 AC26
IO_L3P_T0_DQS_13 AE25
IO_L3N_T0_DQS_13 AE26
IO_L4P_T0_13 AD25
IO_L4N_T0_13 AD26
IO_L5P_T0_13 AF24
IO_L5N_T0_13 AF25
IO_L6P_T0_13 AA24
IO_L6N_T0_VREF_13 AB24
IO_L7P_T1_13 AE22
IO_L7N_T1_13 AF22
IO_L8P_T1_13 AE23
IO_L8N_T1_13 AF23
IO_L9P_T1_DQS_13 AB21
IO_L9N_T1_DQS_13 AB22
IO_L10P_T1_13 AA22
IO_L10N_T1_13 AA23
IO_L11P_T1_SRCC_13 AD23
IO_L11N_T1_SRCC_13 AD24
IO_L12P_T1_MRCC_13 AC23
IO_L12N_T1_MRCC_13 AC24
IO_L13P_T2_MRCC_13 AD20
IO_L13N_T2_MRCC_13 AD21
IO_L14P_T2_SRCC_13 AC21
IO_L14N_T2_SRCC_13 AC22
IO_L15P_T2_DQS_13 AF19
IO_L15N_T2_DQS_13 AF20
IO_L16P_T2_13 AE20
IO_L16N_T2_13 AE21
IO_L17P_T2_13 AD18
IO_L17N_T2_13 AD19
IO_L18P_T2_13 AE18
IO_L18N_T2_13 AF18
IO_L19P_T3_13 W20
IO_L19N_T3_VREF_13 Y20
IO_L20P_T3_13 AA20
IO_L20N_T3_13 AB20
IO_L21P_T3_DQS_13 AC18
IO_L21N_T3_DQS_13 AC19
IO_L22P_T3_13 AA19
IO_L22N_T3_13 AB19
IO_L23P_T3_13 W18
IO_L23N_T3_13 W19
IO_L24P_T3_13 Y18
IO_L24N_T3_13 AA18
IO_25_13 V18
XC7Z045-2FBG676C
IO_0_13
IO_L1P_T0_13
IO_L1N_T0_13
IO_L2P_T0_13
IO_L2N_T0_13
IO_L3P_T0_DQS_13
IO_L3N_T0_DQS_13
IO_L4P_T0_13
IO_L4N_T0_13
IO_L5P_T0_13
IO_L5N_T0_13
IO_L6P_T0_13
IO_L6N_T0_VREF_13
IO_L7P_T1_13
IO_L7N_T1_13
IO_L8P_T1_13
IO_L8N_T1_13
IO_L9P_T1_DQS_13
IO_L9N_T1_DQS_13
IO_L10P_T1_13
IO_L10N_T1_13
IO_L11P_T1_SRCC_13
IO_L11N_T1_SRCC_13
IO_L12P_T1_MRCC_13
IO_L12N_T1_MRCC_13
IO_L13P_T2_MRCC_13
IO_L13N_T2_MRCC_13
IO_L14P_T2_SRCC_13
IO_L14N_T2_SRCC_13
IO_L15P_T2_DQS_13
IO_L15N_T2_DQS_13
IO_L16P_T2_13
IO_L16N_T2_13
IO_L17P_T2_13
IO_L17N_T2_13
IO_L18P_T2_13
IO_L18N_T2_13
IO_L19P_T3_13
IO_L19N_T3_VREF_13
IO_L20P_T3_13
IO_L20N_T3_13
IO_L21P_T3_DQS_13
IO_L21N_T3_DQS_13
IO_L22P_T3_13
IO_L22N_T3_13
IO_L23P_T3_13
IO_L23N_T3_13
IO_L24P_T3_13
IO_L24N_T3_13
IO_25_13
IO_L11P_T1_SRCC_13
IO_L11N_T1_SRCC_13
IO_L12P_T1_MRCC_13
IO_L12N_T1_MRCC_13
IO_L13P_T2_MRCC_13
IO_L13N_T2_MRCC_13
IO_L14P_T2_SRCC_13
IO_L14N_T2_SRCC_13
IO_L15P_T2_DQS_13
IO_L15N_T2_DQS_13

BANK13


DD1F
BANK 35
IO_0_VRN_35 H16
IO_L1P_T0_AD0P_35 E12
IO_L1N_T0_AD0N_35 E12
IO_L2P_T0_AD8P_35 E10
IO_L2N_T0_AD8N_35 D10
IO_L3P_T0_DQS_AD1P_35 G10
IO_L3N_T0_DQS_AD1N_35 F10
IO_L4P_T0_35 E11
IO_L4N_T0_35 D11
IO_L5P_T0_AD9P_35 G12
IO_L5N_T0_AD9N_35 G11
IO_L6P_T0_35 F13
IO_L6N_T0_VREF_35 E13
IO_L7P_T1_AD2P_35 H13
IO_L7N_T1_AD2N_35 H12
IO_L8P_T1_AD10P_35 K13
IO_L8N_T1_AD10N_35 J13
IO_L9P_T1_DQS_AD3P_35 K15
IO_L9N_T1_DQS_AD3N_35 J15
IO_L10P_T1_AD11P_35 G16
IO_L10N_T1_AD11N_35 G15
IO_L11P_T1_SRCC_35 G14
IO_L11N_T1_SRCC_35 F14
IO_L12P_T1_MRCC_35 J14 CLKPL_P
IO_L12N_T1_MRCC_35 H14 CLKPL_N
IO_L13P_T2_MRCC_35 D15
IO_L13N_T2_MRCC_35 D14
IO_L14P_T2_AD4P_SRCC_35 F15
IO_L14N_T2_AD4N_SRCC_35 E15
IO_L15P_T2_DQS_AD12P_35 C17
IO_L15N_T2_DQS_AD12N_35 C16
IO_L16P_T2_35 E16
IO_L16N_T2_35 D16
IO_L17P_T2_AD5P_35 B16
IO_L17N_T2_AD5N_35 B15
IO_L18P_T2_AD13P_35 B17
IO_L18N_T2_AD13N_35 A17
IO_L19P_T3_35 D13
IO_L19N_T3_VREF_35 C13
IO_L20P_T3_AD6P_35 C14
IO_L20N_T3_AD6N_35 B14
IO_L21P_T3_DQS_AD14P_35 A15
IO_L21N_T3_DQS_AD14N_35 A14
IO_L22P_T3_AD7P_35 C12
IO_L22N_T3_AD7N_35 B12
IO_L23P_T3_35 C11
IO_L23N_T3_35 B11
IO_L24P_T3_AD15P_35 A13
IO_L24N_T3_AD15N_35 A12
IO_25_VRP_35 K12
XC7Z045-2FBG676C
IO_L11P_T1_SRCC_35
IO_L11N_T1_SRCC_35
IO_L13P_T2_MRCC_35
IO_L13N_T2_MRCC_35
IO_L14P_T2_AD4P_SRCC_35
IO_L14N_T2_AD4N_SRCC_35
R217 100
ZQ5
Out-
Out+
VDD
CLOCK GEN
OE
NC
GND
SiT9102AI-243
D3.3V
C252 0.1u
DGND
BANK35


DGND
C443 C444 C445
1u 1u 1u
VCCINT_D1.0V
C259 C260 C261 C262 C263 C264 C265 C266 C267 C268 C269 C270 C271 C272
0.1u
DGND
VCCINT_D1.0V
C273 C274 C275 C276
0.1u
DGND
DGND
C442
VCCPINT_D1.0V
1u
C277 C278 C279 C280 C281 C282
0.1u
DGND
VCC_P_AUX_D1.8V
C283 C284 C285 C286 C287 C288
0.1u
DGND
MGTAVCC_D1.0V
C289 C290 C291 C292 C293 C294 C295 C296 C297 C298
0.1u
DGND
MGTAVTT_D1.2V
C299 C300 C301 C302 C303 C304 C305 C306 C307 C308
0.1u
DGND
VCC_P_AUX_D1.8V
C309 C310 C311 C312
0.1u
DGND
VCCAUX_IO_D2.0V
C313 C314 C315
0.1u
DGND
LDO_D1.8V
C316 C317 C318
0.1u
DGND
VCCBATT
C319
0.1u
DGND
VCCO_12
C320 C321 C322 C323 C324 C325
0.1u
DGND
VCCO_13
C326 C327 C328 C329 C330 C331
0.1u
DGND
VCCO_35
C332 C333 C334 C335 C336 C337
0.1u
DGND

CAPACITORS