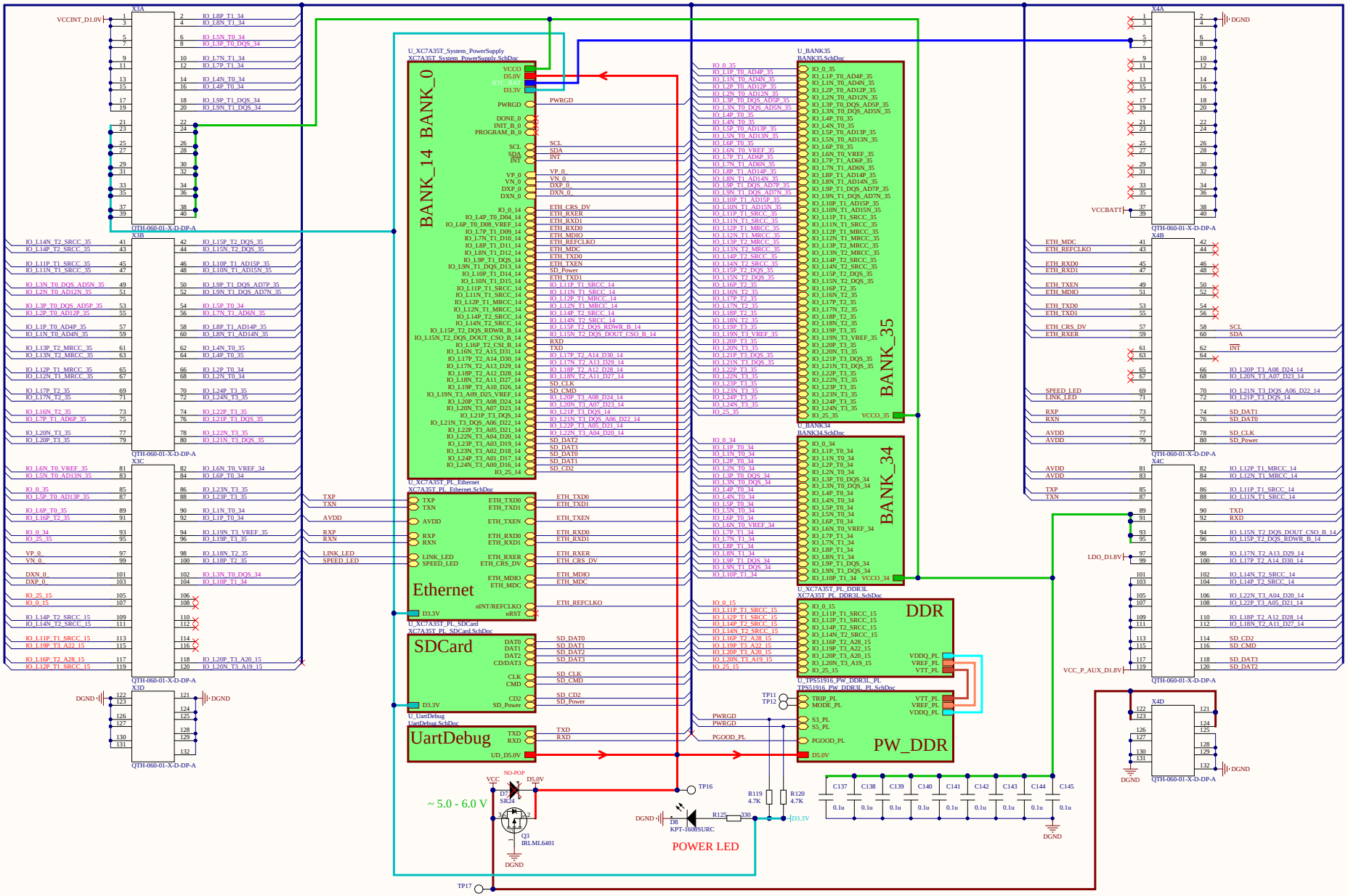
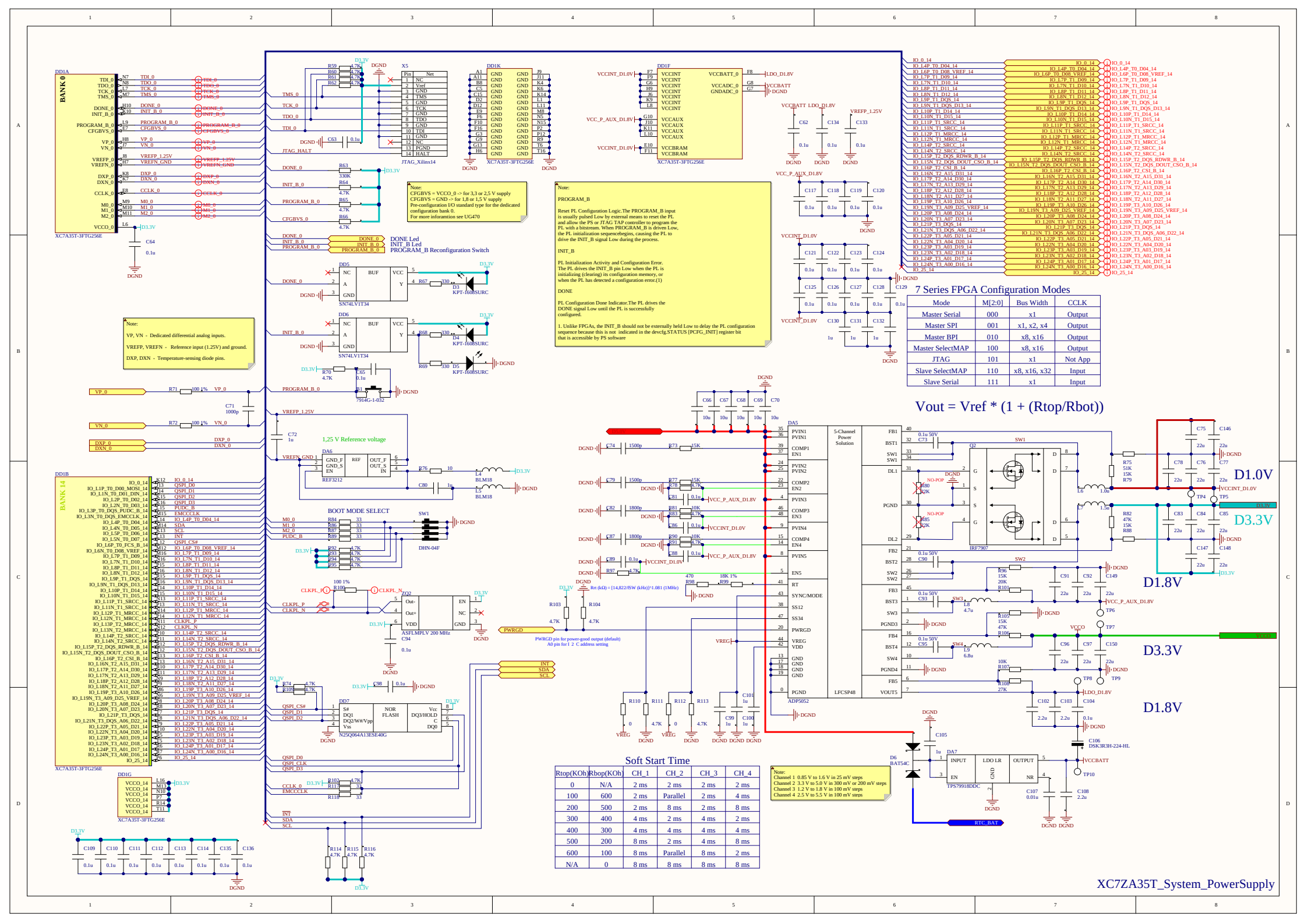
SI-XC7A35T-SOM-QTH





Note:
VP, VN - Dedicated differential analog inputs.
VREFP, VREFN - Reference input (1.25V) and ground.
DXP, DXN - Temperature-sensing diode pins.

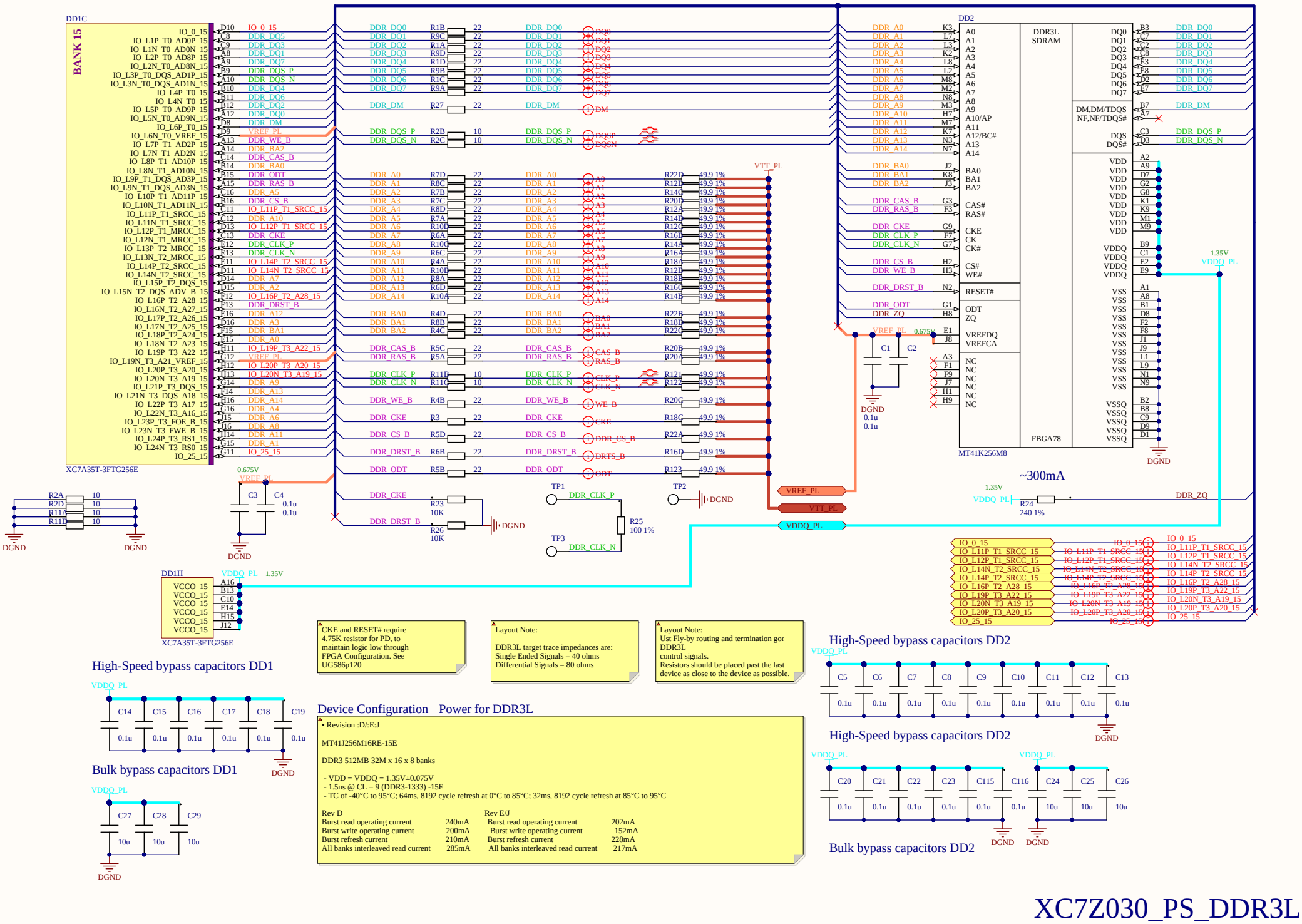
Note:
CFGBVS = VCCO_0 -> for 3,3 or 2,5 V supply
CFGBVS = GND -> for 1,8 or 1,5 V supply
Pre-configuration I/O standard type for the dedicated configuration bank 0.
For more inforamtion see UG470

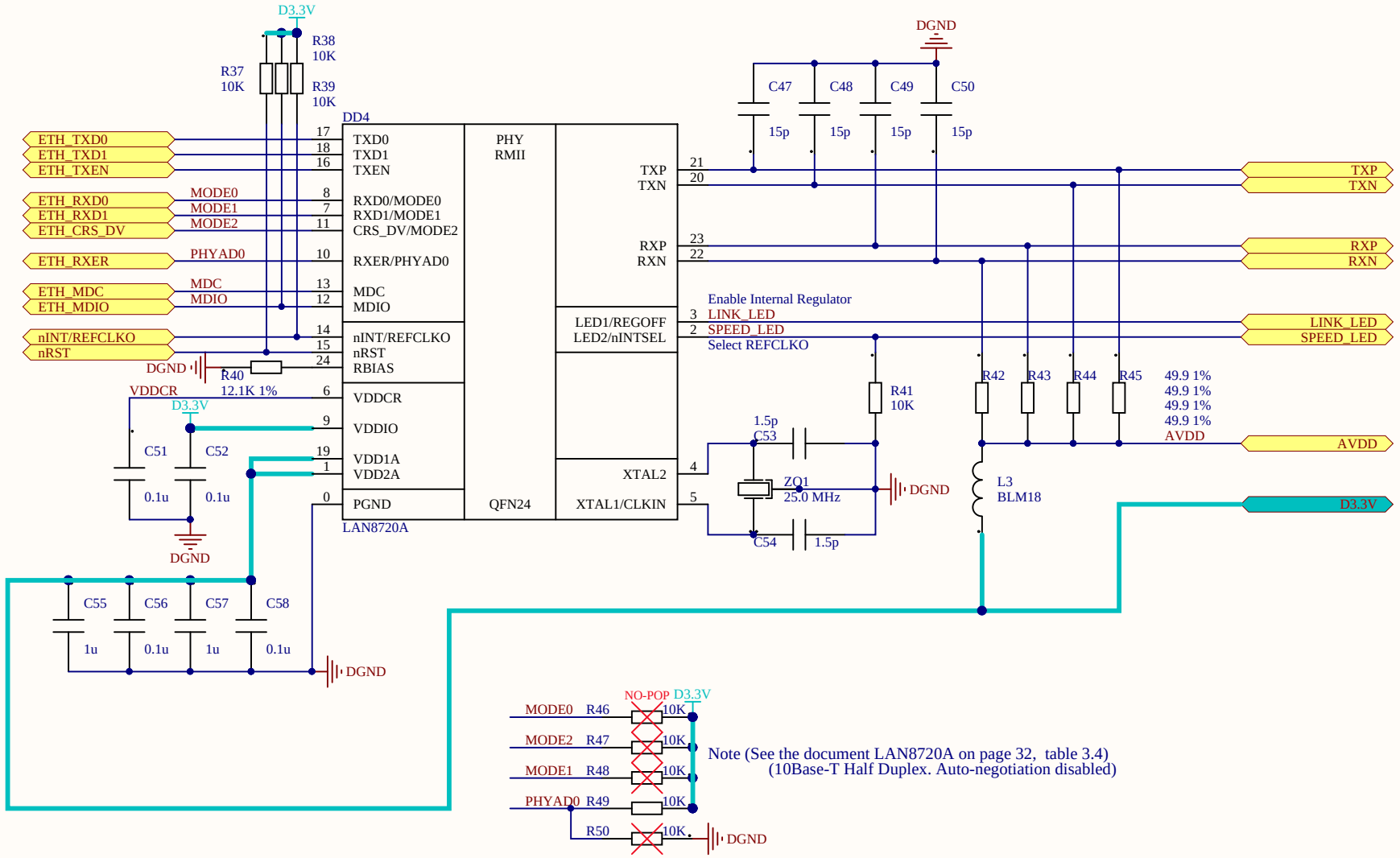
Note:
PROGRAM_B
Reset PL Configuration Logic.The PROGRAM_B input is usually pulsed Low by external means to reset the PL and allow the PS or JTAG TAP controller to program the PL with a bitstream. When PROGRAM_B is driven Low, the PL initialization sequencebegins, causing the PL to drive the INIT_B signal Low during the process.
INIT_B
PL Initialization Activity and Configuration Error. The PL drives the INIT_B pin Low when the PL is initializing (clearing) its configuration memory, or when the PL has detected a configuration error.(1)
DONE
PL Configuration Done Indicator.The PL drives the DONE signal Low until the PL is successfully configured.
1. Unlike FPGAs, the INIT_B should not be externally held Low to delay the PL configuration sequence because this is not indicated in the devcfg.STATUS [PCFG_INIT] register bit that is accessible by PS software

Mode	M[2:0]	Bus Width	CCLK
Master Serial	000	x1	Output
Master SPI	001	x1, x2, x4	Output
Master BPI	010	x8, x16	Output
Master SelectMAP	100	x8, x16	Output
JTAG	101	x1	Not App
Slave SelectMAP	110	x8, x16, x32	Input
Slave Serial	111	x1	Input

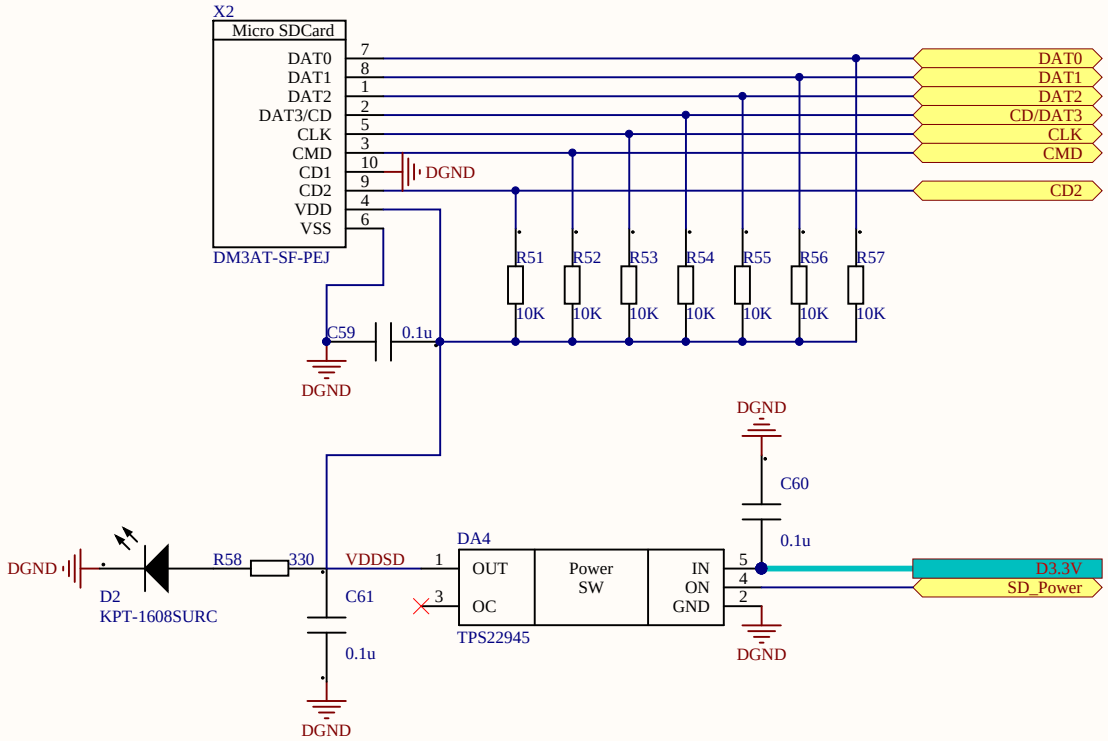
Rtop(KOh)	Rbop(KOh)	CH_1	CH_2	CH_3	CH_4
0	N/A	2 ms	2 ms	2 ms	2 ms
100	600	2 ms	Parallel	2 ms	4 ms
200	500	2 ms	8 ms	2 ms	8 ms
300	400	4 ms	2 ms	4 ms	2 ms
400	300	4 ms	4 ms	4 ms	4 ms
500	200	8 ms	2 ms	4 ms	8 ms
600	100	8 ms	Parallel	8 ms	2 ms
N/A	0	8 ms	8 ms	8 ms	8 ms

Note:
Channel 1 0.85 V to 1.6 V in 25 mV steps
Channel 2 3.3 V to 5.0 V in 300 mV or 200 mV steps
Channel 3 1.2 V to 1.8 V in 100 mV steps
Channel 4 2.5 V to 5.5 V in 100 mV steps

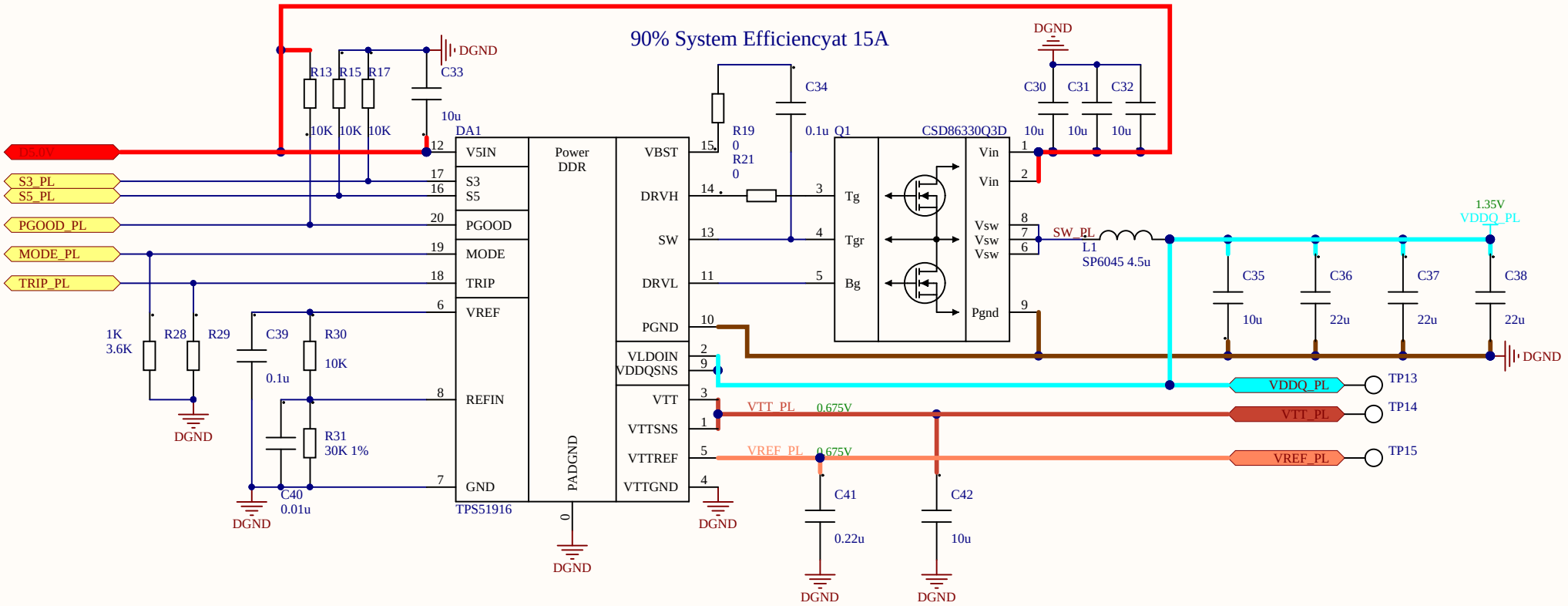

DD1C
BANK 15
XC7A35T-3FTG256E
DD2
DDR3L SDRAM
FBGA78
MT41K256M8
DD1H
XC7A35T-3FTG256E
VTT_PL
VREF_PL
VDDQ_PL
DGND
~300mA
High-Speed bypass capacitors DD1
Bulk bypass capacitors DD1
High-Speed bypass capacitors DD2
High-Speed bypass capacitors DD2
Bulk bypass capacitors DD2
CKE and RESET# require 4.75K resistor for PD, to maintain logic low through FPGA Configuration. See UG586p120
Layout Note:
DDR3L target trace impedances are:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms
Layout Note:
Ust Fly-by routing and termination gor DDR3L
control signals.
Resistors should be placed past the last device as close to the device as possible.
Device Configuration Power for DDR3L
• Revision :D/:E:J
MT41J256M16RE-15E
DDR3 512MB 32M x 16 x 8 banks
- VDD = VDDQ = 1.35V±0.075V
- 1.5ns @ CL = 9 (DDR3-1333) -15E
- TC of -40°C to 95°C; 64ms, 8192 cycle refresh at 0°C to 85°C; 32ms, 8192 cycle refresh at 85°C to 95°C
Rev D
Burst read operating current 240mA
Burst write operating current 200mA
Burst refresh current 210mA
All banks interleaved read current 285mA
Rev E/J
Burst read operating current 202mA
Burst write operating current 152mA
Burst refresh current 228mA
All banks interleaved read current 217mA
XC7Z030_PS_DDR3L



XC7A35T_PL_Ethernet



XC7A35T_PL_SDCard



Device Configuration for DDR3/3L

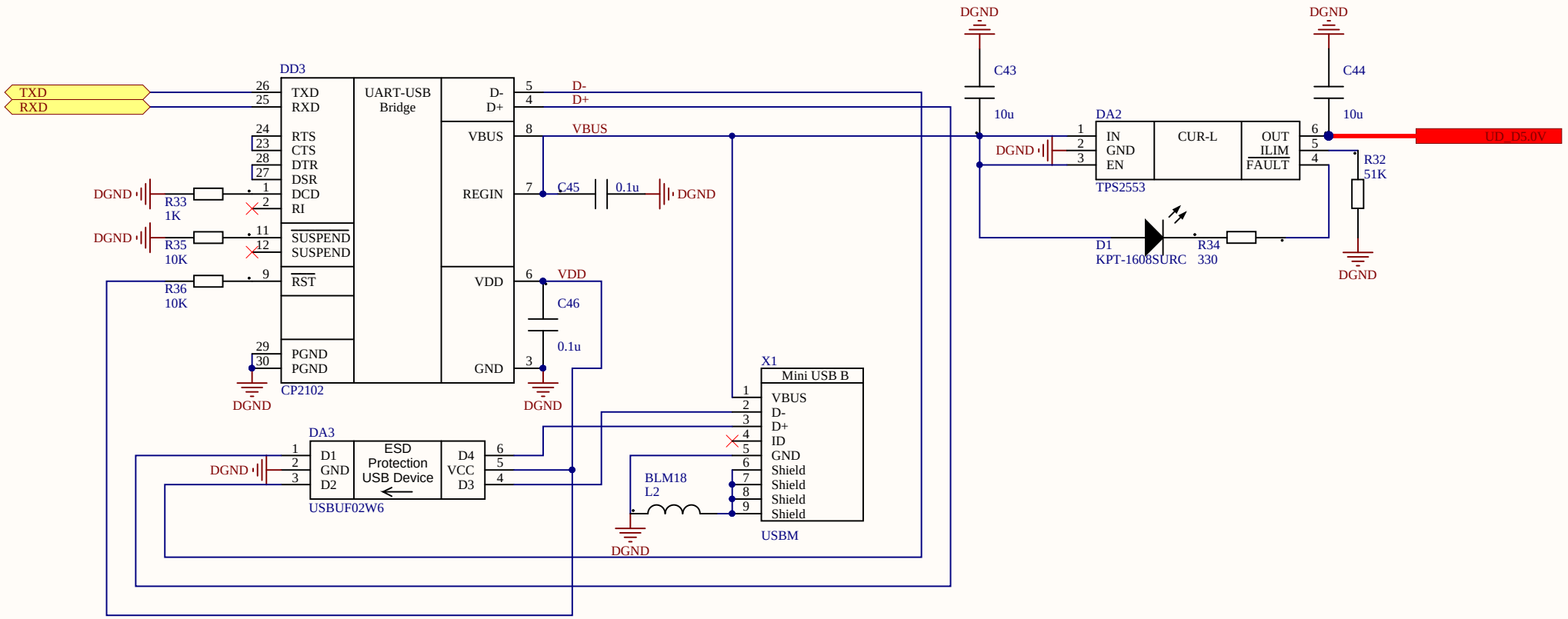
MODE: R = 1K Fsw = 500KHz
TRIP: CDS86350Q5D Rds = 2mO Iocl = 2.5A Rtrip = 3.6K

Vin = 5.5V VDDQ = 1.35V VTT = 0.675V

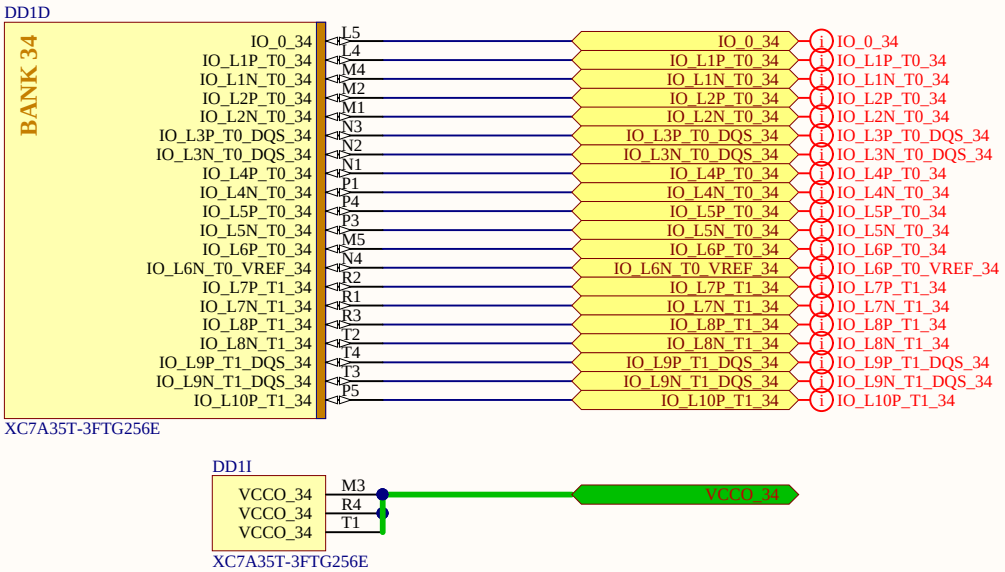
Iout = 1.8A Iind(ripple) = 0.6A Iind(peak) = 2.75A Ivtt = 1.2A

Cout > 57u

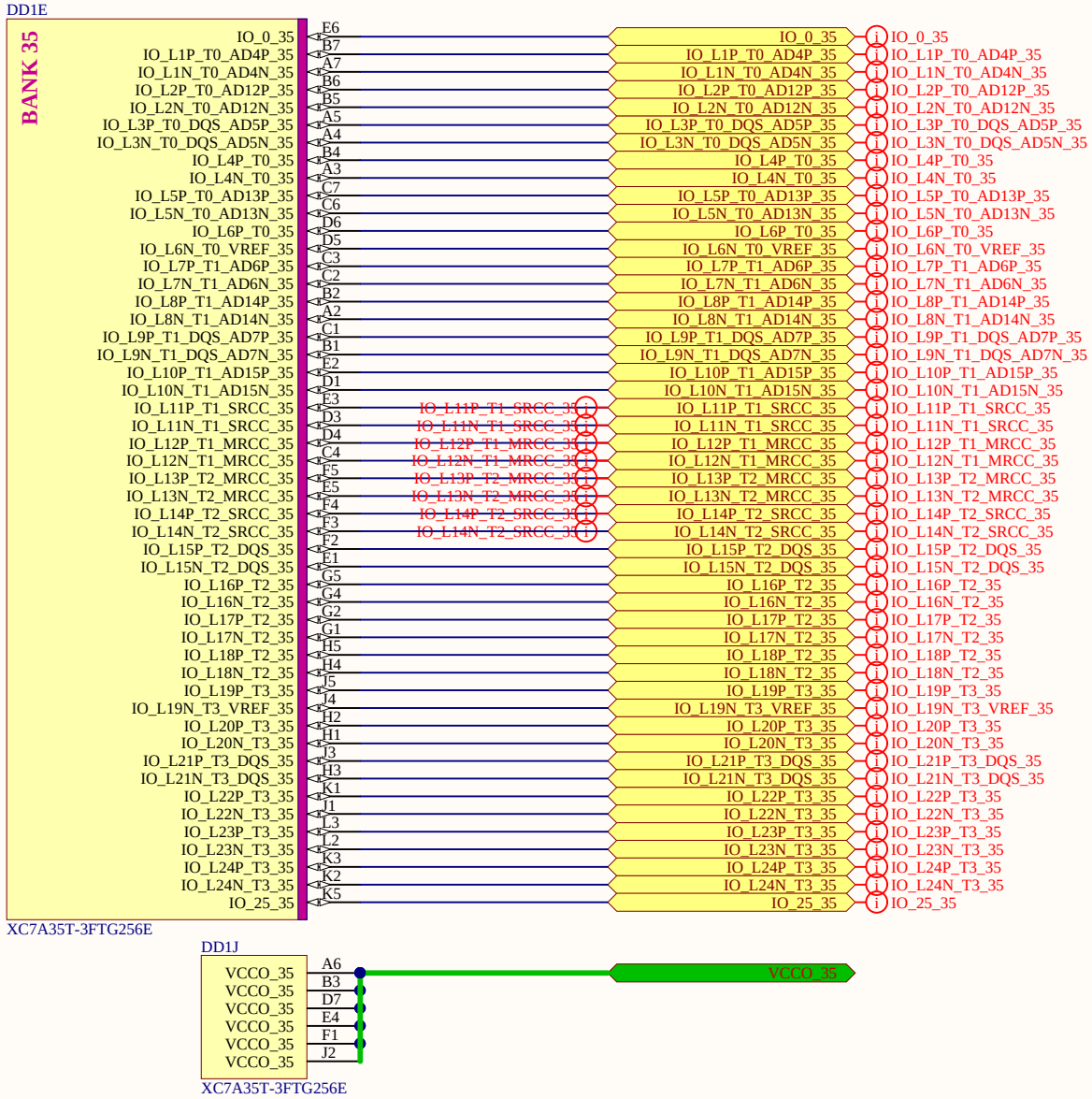
TPS51916_PW_DDR3L_PL


TXD
RXD
DD3
26
25
TXD
RXD
UART-USB
Bridge
D-
D+
5
4
D-
D+
24
23
28
27
1
2
RTS
CTS
DTR
DSR
DCD
RI
VBUS
8
VBUS
DGND
R33
1K
DGND
R35
10K
11
12
SUSPEND
SUSPEND
REGIN
7
C45
0.1u
DGND
DGND
R36
10K
9
RST
VDD
6
VDD
C46
0.1u
29
30
PGND
PGND
GND
3
DGND
DGND
CP2102
X1
Mini USB B
1
2
3
4
5
6
7
8
9
VBUS
D-
D+
ID
GND
Shield
Shield
Shield
Shield
DA3
1
2
3
D1
GND
D2
ESD
Protection
USB Device
D4
VCC
D3
6
5
4
DGND
USBUF02W6
BLM18
L2
DGND
USBM
DGND
C43
10u
DGND
DA2
1
2
3
IN
GND
EN
CUR-L
OUT
ILIM
FAULT
6
5
4
TPS2553
DGND
C44
10u
UD_D5.0V
R32
51K
DGND
D1
KPT-1608SURC
R34
330

UartDebug


DD1D
BANK 34
IO_0_34
IO_L1P_T0_34
IO_L1N_T0_34
IO_L2P_T0_34
IO_L2N_T0_34
IO_L3P_T0_DQS_34
IO_L3N_T0_DQS_34
IO_L4P_T0_34
IO_L4N_T0_34
IO_L5P_T0_34
IO_L5N_T0_34
IO_L6P_T0_34
IO_L6N_T0_VREF_34
IO_L7P_T1_34
IO_L7N_T1_34
IO_L8P_T1_34
IO_L8N_T1_34
IO_L9P_T1_DQS_34
IO_L9N_T1_DQS_34
IO_L10P_T1_34
L5
L4
M4
M2
M1
N3
N2
N1
P1
P4
P3
M5
N4
R2
R1
R3
T2
T4
T3
P5
XC7A35T-3FTG256E
DD1I
VCCO_34
VCCO_34
VCCO_34
M3
R4
T1
XC7A35T-3FTG256E

BANK34


DD1E
BANK 35
IO_0_35 E6
IO_L1P_T0_AD4P_35 B7
IO_L1N_T0_AD4N_35 A7
IO_L2P_T0_AD12P_35 B6
IO_L2N_T0_AD12N_35 B5
IO_L3P_T0_DQS_AD5P_35 A5
IO_L3N_T0_DQS_AD5N_35 A4
IO_L4P_T0_35 B4
IO_L4N_T0_35 A3
IO_L5P_T0_AD13P_35 C7
IO_L5N_T0_AD13N_35 C6
IO_L6P_T0_35 D6
IO_L6N_T0_VREF_35 D5
IO_L7P_T1_AD6P_35 C3
IO_L7N_T1_AD6N_35 C2
IO_L8P_T1_AD14P_35 B2
IO_L8N_T1_AD14N_35 A2
IO_L9P_T1_DQS_AD7P_35 C1
IO_L9N_T1_DQS_AD7N_35 B1
IO_L10P_T1_AD15P_35 E2
IO_L10N_T1_AD15N_35 D1
IO_L11P_T1_SRCC_35 E3
IO_L11N_T1_SRCC_35 D3
IO_L12P_T1_MRCC_35 D4
IO_L12N_T1_MRCC_35 C4
IO_L13P_T2_MRCC_35 F5
IO_L13N_T2_MRCC_35 E5
IO_L14P_T2_SRCC_35 F4
IO_L14N_T2_SRCC_35 F3
IO_L15P_T2_DQS_35 F2
IO_L15N_T2_DQS_35 E1
IO_L16P_T2_35 G5
IO_L16N_T2_35 G4
IO_L17P_T2_35 G2
IO_L17N_T2_35 G1
IO_L18P_T2_35 H5
IO_L18N_T2_35 H4
IO_L19P_T3_35 J5
IO_L19N_T3_VREF_35 J4
IO_L20P_T3_35 H2
IO_L20N_T3_35 H1
IO_L21P_T3_DQS_35 J3
IO_L21N_T3_DQS_35 H3
IO_L22P_T3_35 K1
IO_L22N_T3_35 J1
IO_L23P_T3_35 L3
IO_L23N_T3_35 L2
IO_L24P_T3_35 K3
IO_L24N_T3_35 K2
IO_25_35 K5
XC7A35T-3FTG256E
DD1J
VCCO_35 A6
VCCO_35 B3
VCCO_35 D7
VCCO_35 E4
VCCO_35 F1
VCCO_35 J2
XC7A35T-3FTG256E
VCCO_35
BANK35