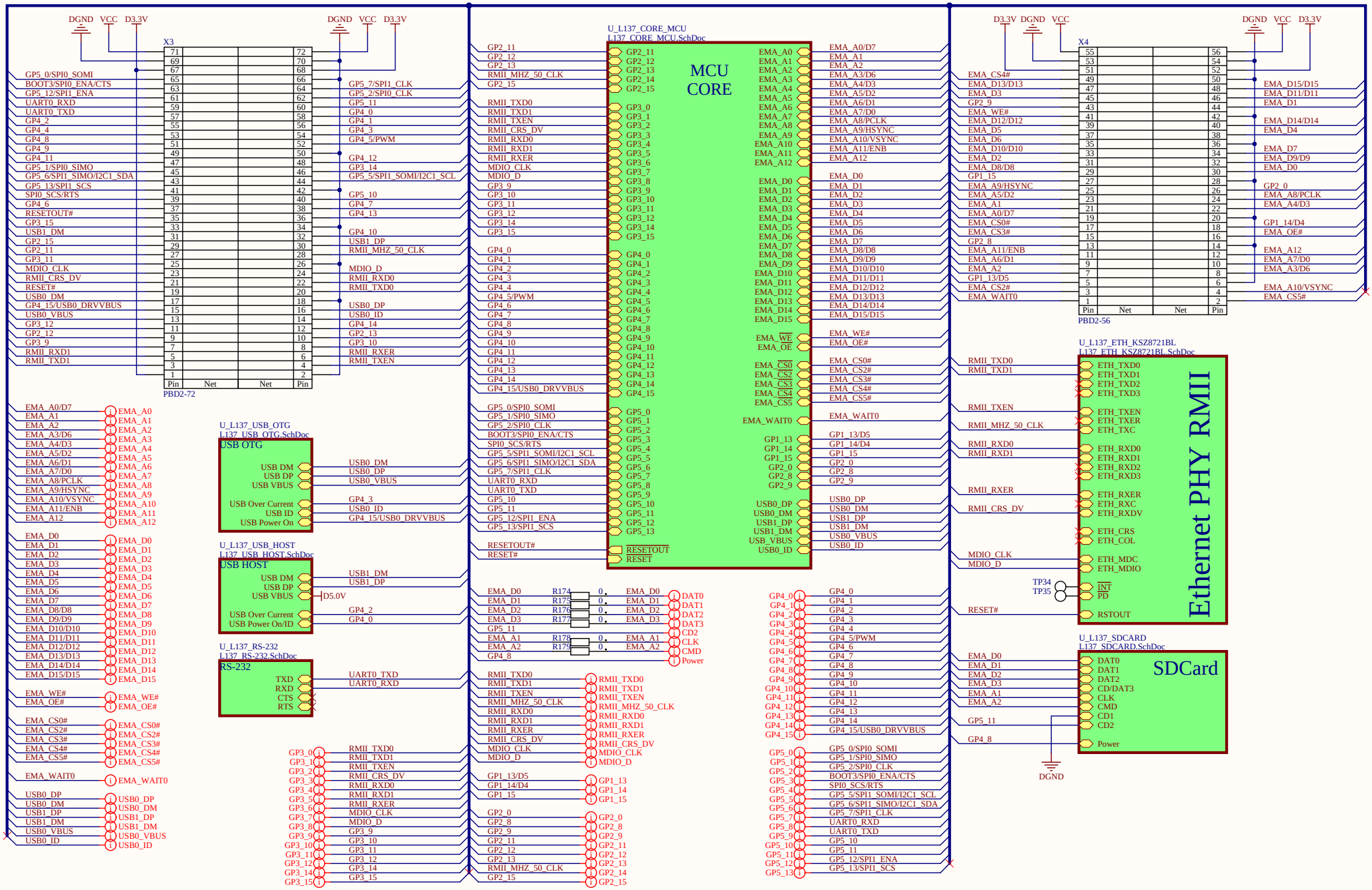
SI-L137-SBC-PBD2



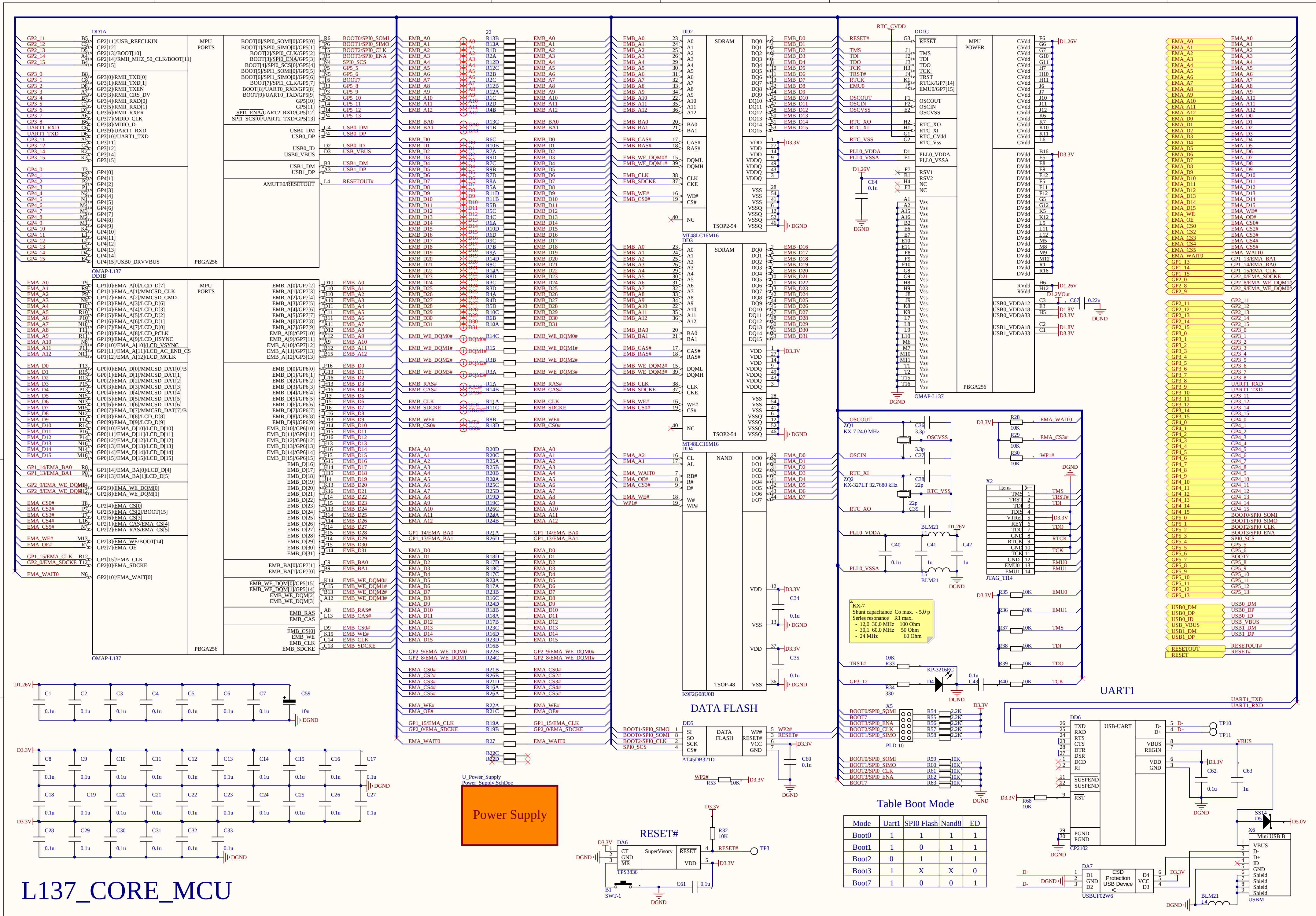
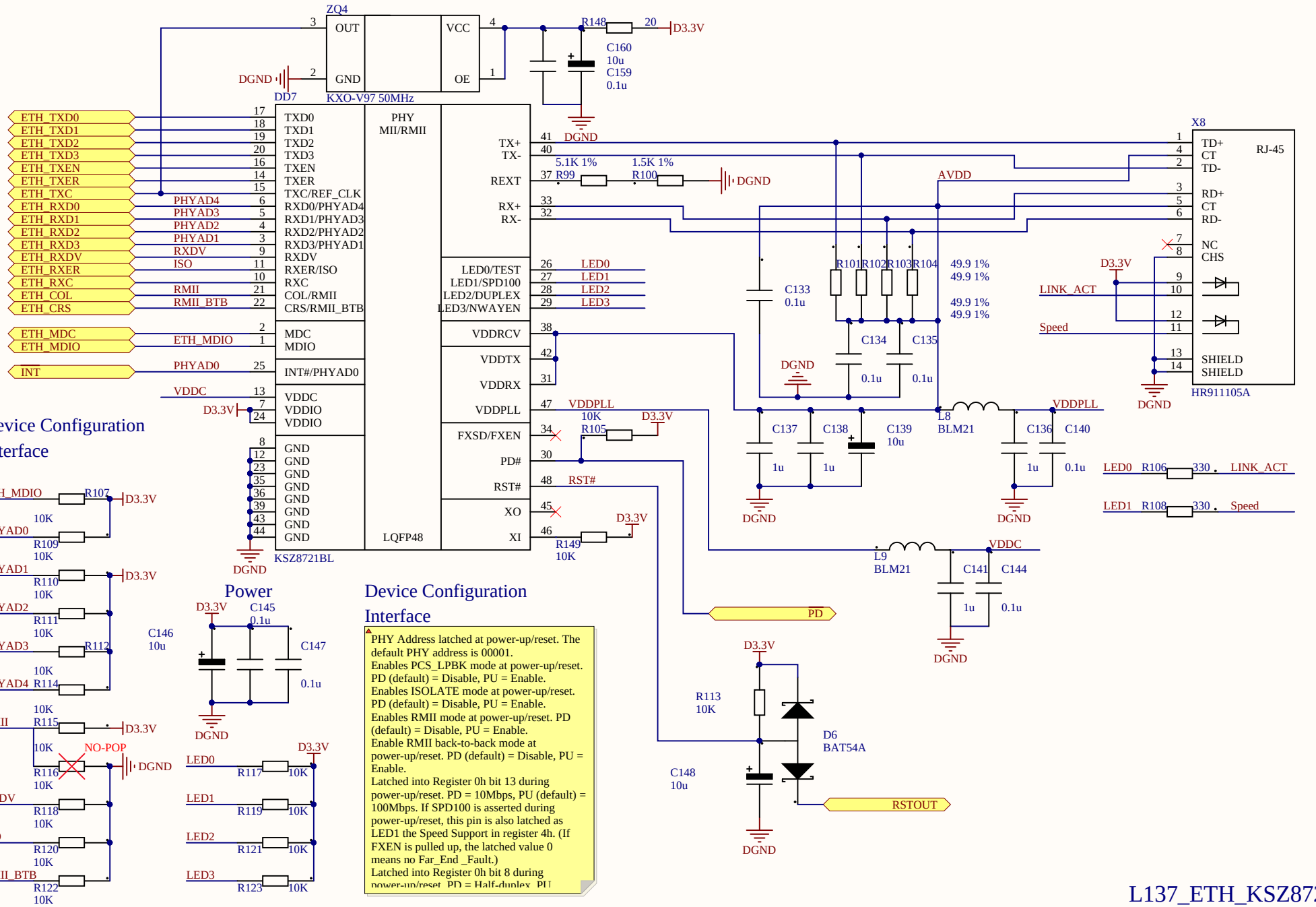
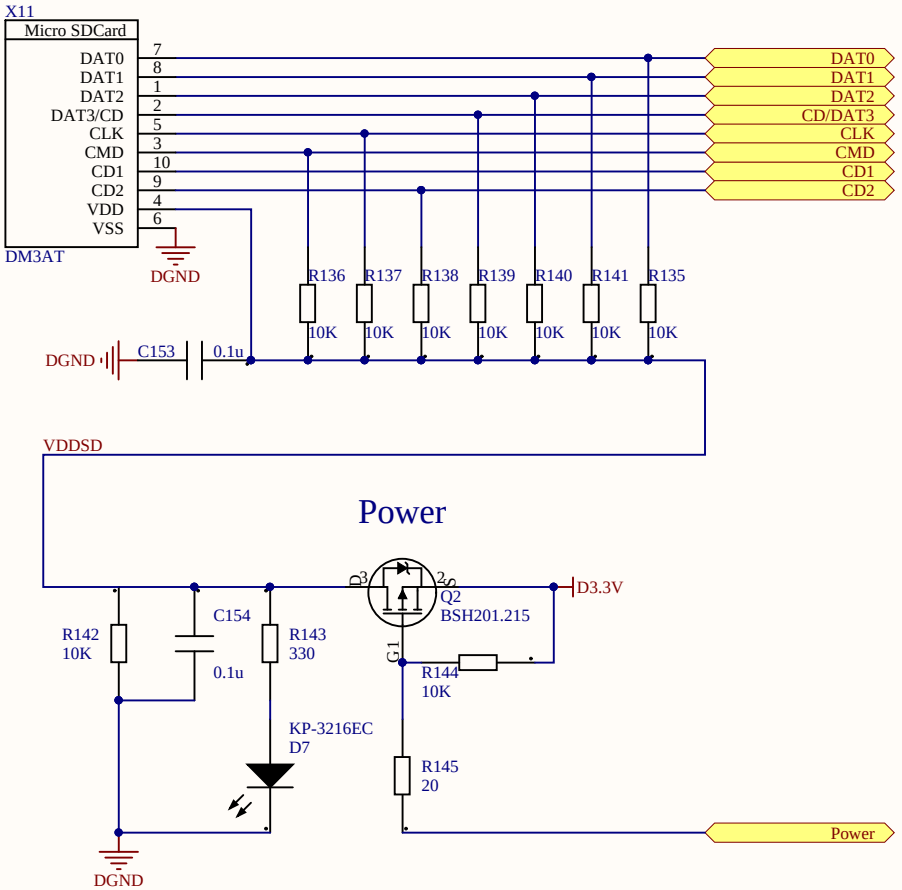


Table Boot Mode

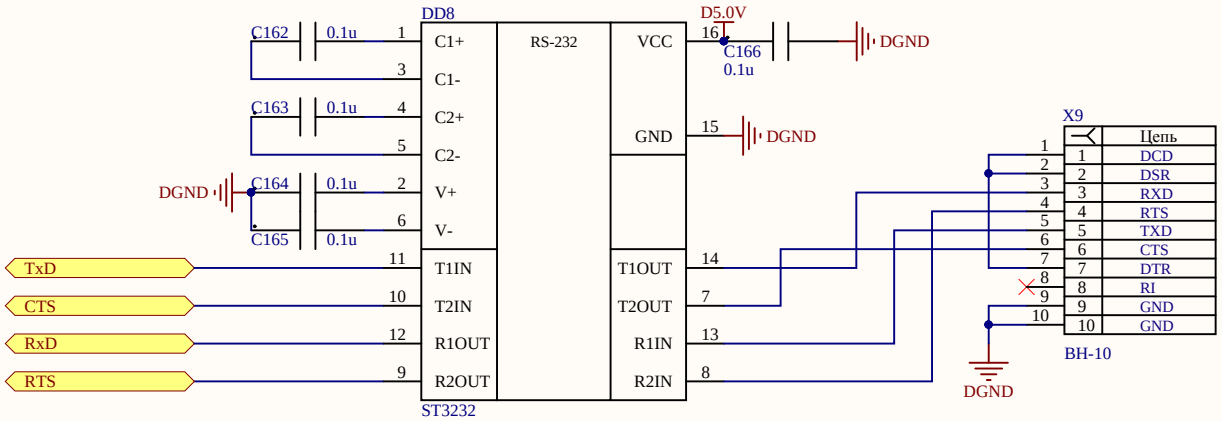
Mode	Uart1	SPI0 Flash	Nand8	ED
Boot0	1	1	1	1
Boot1	1	0	1	1
Boot2	0	1	1	1
Boot3	1	X	X	0
Boot7	1	0	0	1


ZQ4
OUT
GND
VCC
OE
KXO-V97 50MHz
DD7
R148
C160
10u
C159
0.1u
D3.3V
DGND
ETH_TXD0
ETH_TXD1
ETH_TXD2
ETH_TXD3
ETH_TXEN
ETH_TXER
ETH_TXC
ETH_RXD0
ETH_RXD1
ETH_RXD2
ETH_RXD3
ETH_RXDV
ETH_RXER
ETH_RXC
ETH_COL
ETH_CRS
ETH_MDC
ETH_MDIO
INT
PHYAD4
PHYAD3
PHYAD2
PHYAD1
RXDV
ISO
RMII
RMII_BTB
PHYAD0
VDDC
TXD0
TXD1
TXD2
TXD3
TXEN
TXER
TXC/REF_CLK
RXD0/PHYAD4
RXD1/PHYAD3
RXD2/PHYAD2
RXD3/PHYAD1
RXDV
RXER/ISO
RXC
COL/RMII
CRS/RMII_BTB
MDC
MDIO
INT#/PHYAD0
VDDC
VDDIO
VDDIO
GND
PHY
MII/RMII
LQFP48
KSZ8721BL
TX+
TX-
REXT
RX+
RX-
LED0/TEST
LED1/SPD100
LED2/DUPLEX
LED3/NWAYEN
VDDRCV
VDDTX
VDDRX
VDDPLL
FXSD/FXEN
PD#
RST#
XO
XI
R99
5.1K 1%
R100
1.5K 1%
AVDD
R101
R102
R103
R104
49.9 1%
C133
0.1u
C134
C135
0.1u
0.1u
LED0
LED1
LED2
LED3
X8
RJ-45
TD+
CT
TD-
RD+
CT
RD-
NC
CHS
SHIELD
SHIELD
HR911105A
LINK_ACT
Speed
R105
10K
R149
10K
RST#
PD
VDDPLL
L8
BLM21
C136
C140
C137
C138
C139
10u
1u
1u
1u
0.1u
L9
BLM21
C141
C144
1u
0.1u
VDDC
LED0
R106
330
LINK_ACT
LED1
R108
330
Speed
Device Configuration
Interface
ETH_MDIO
R107
10K
PHYAD0
R109
10K
PHYAD1
R110
10K
PHYAD2
R111
10K
PHYAD3
R112
10K
PHYAD4
R114
10K
RMII
R115
10K
NO-POP
R116
10K
RXDV
R118
10K
ISO
R120
10K
RMII_BTB
R122
10K
Power
C145
0.1u
C146
10u
C147
0.1u
LED0
R117
10K
LED1
R119
10K
LED2
R121
10K
LED3
R123
10K
Device Configuration
Interface
PHY Address latched at power-up/reset. The default PHY address is 00001.
Enables PCS_LPBK mode at power-up/reset. PD (default) = Disable, PU = Enable.
Enables ISOLATE mode at power-up/reset. PD (default) = Disable, PU = Enable.
Enables RMII mode at power-up/reset. PD (default) = Disable, PU = Enable.
Enable RMII back-to-back mode at power-up/reset. PD (default) = Disable, PU = Enable.
Latched into Register 0h bit 13 during power-up/reset. PD = 10Mbps, PU (default) = 100Mbps. If SPD100 is asserted during power-up/reset, this pin is also latched as LED1 the Speed Support in register 4h. (If FXEN is pulled up, the latched value 0 means no Far_End _Fault.)
Latched into Register 0h bit 8 during power-up/reset. PD = Half-duplex, PU
R113
10K
D6
BAT54A
C148
10u
RSTOUT
L137_ETH_KSZ8721BL

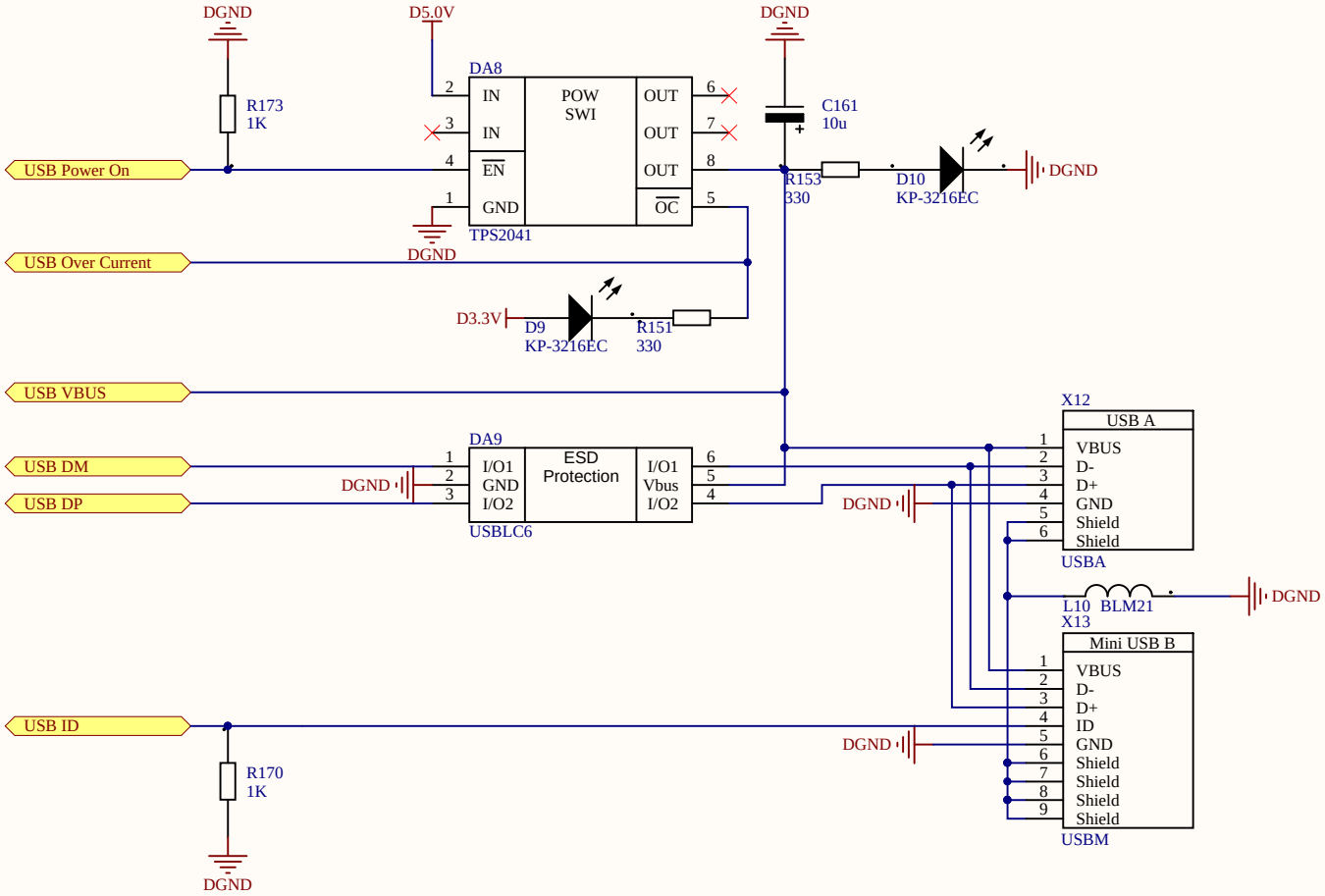
L137_SDCard

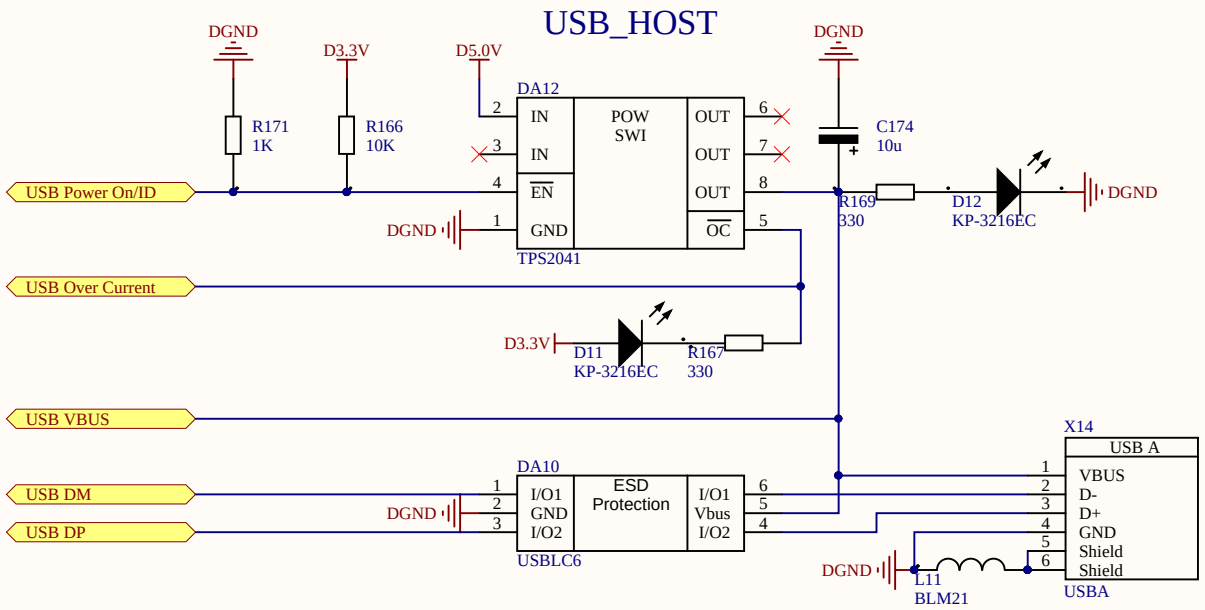

X11
Micro SDCard
DAT0
DAT1
DAT2
DAT3/CD
CLK
CMD
CD1
CD2
VDD
VSS
7
8
1
2
5
3
10
9
4
6
DM3AT
DGND
DAT0
DAT1
DAT2
CD/DAT3
CLK
CMD
CD1
CD2
R136
R137
R138
R139
R140
R141
R135
10K
DGND
C153
0.1u
VDDSD
Power
D3
Q2
BSH201.215
D3.3V
R142
10K
C154
0.1u
R143
330
R144
10K
KP-3216EC
D7
R145
20
Power
DGND

L137_RS-232


DD8
C162
0.1u
C163
0.1u
C164
0.1u
C165
0.1u
DGND
C1+
C1-
C2+
C2-
V+
V-
RS-232
VCC
GND
T1IN
T2IN
R1OUT
R2OUT
T1OUT
T2OUT
R1IN
R2IN
ST3232
D5.0V
C166
0.1u
DGND
DGND
TxD
CTS
RxD
RTS
X9
Цепь
DCD
DSR
RXD
RTS
TXD
CTS
DTR
RI
GND
GND
BH-10
DGND

L137_USB_OTG


DGND
D5.0V
DGND
DA8
R173
1K
IN
IN
EN
GND
POW
SWI
OUT
OUT
OUT
OC
C161
10u
USB Power On
R153
330
D10
KP-3216EC
DGND
TPS2041
DGND
USB Over Current
D3.3V
D9
KP-3216EC
R151
330
USB VBUS
X12
USB A
VBUS
D-
D+
GND
Shield
Shield
USBA
DA9
USB DM
USB DP
DGND
I/O1
GND
I/O2
ESD
Protection
I/O1
Vbus
I/O2
USBLC6
DGND
L10 BLM21
DGND
X13
Mini USB B
VBUS
D-
D+
ID
GND
Shield
Shield
Shield
Shield
USBM
USB ID
DGND
R170
1K
DGND


USB_HOST
DGND
D3.3V
D5.0V
DGND
R171
1K
R166
10K
DA12
IN
IN
EN
GND
POW
SWI
OUT
OUT
OUT
OC
TPS2041
C174
10u
USB Power On/ID
USB Over Current
USB VBUS
USB DM
USB DP
R169
330
D12
KP-3216EC
DGND
D3.3V
D11
KP-3216EC
R167
330
DA10
I/O1
GND
I/O2
ESD
Protection
I/O1
Vbus
I/O2
USBLC6
X14
USB A
VBUS
D-
D+
GND
Shield
Shield
USBA
DGND
L11
BLM21

Power_Supply